NEC

MOS INTEGRATED CIRCUIT

# μPD753204, 753206, 753208

## 4-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD753208 is one of the 75XL Series 4-bit single-chip microcontrollers and has a data processing capability comparable to that of an 8-bit microcontroller.

The μPD753208 has an on-chip LCD controller/driver and is based on the μPD75308B of the 75X Series. However, the μPD75308B is supplied in an 80-pin package, whereas the μPD753208 is supplied in a 48-pin package (375 mils, 0.65-mm pitch) and therefore is suitable for small-scale application systems. In addition, the μPD753208 features expanded CPU functions and performs high-speed operations at a low voltage of 1.8 V.

**Detailed information about functions can be found in the following user's manual. Be sure to read it before designing. μPD753208 User's Manual: U10158E**

### Features

- Low-voltage operation: $V_{DD}$ = 1.8 to 5.5 V
  - Can be driven by two 1.5-V batteries
- Internal memory
  - Program memory (ROM):
    4096 × 8 bits (μPD753204)
    6144 × 8 bits (μPD753206)
    8192 × 8 bits (μPD753208)
  - Data memory (RAM):
    512 × 4 bits
- Variable instruction execution time for high-speed operation and power saving operation
  - 0.95, 1.91, 3.81, 15.3 μs (@ 4.19-MHz operation)
  - 0.67, 1.33, 2.67, 10.7 μs (@ 6.0-MHz operation)
- Internal programmable LCD controller/driver
- Small package:
  48-pin plastic shrink SOP (375 mils, 0.65-mm pitch)
- One-time PROM version: μPD75P3216

### Applications

Remote controllers, Cameras, Sphygnomamometers, Compact-disc radio cassette player compo systems, gas meters, etc.

### Ordering Information

| Part number | Package | ROM (× 8 bits) |
|---|---|---|
| μPD753204GT-××× | 48-pin plastic shrink SOP (375 mils, 0.65-mm pitch) | 4096 |
| μPD753206GT-××× | 48-pin plastic shrink SOP (375 mils, 0.65-mm pitch) | 6144 |
| μPD753208GT-××× | 48-pin plastic shrink SOP (375 mils, 0.65-mm pitch) | 8192 |

**Remark** ××× indicates ROM code suffix.

**Unless otherwise specified, references in this data sheet to the μPD753208 mean the μPD753204 and the μPD753206.**

**The information in this document is subject to change without notice.**

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**The mark ★ shows major revised points.**

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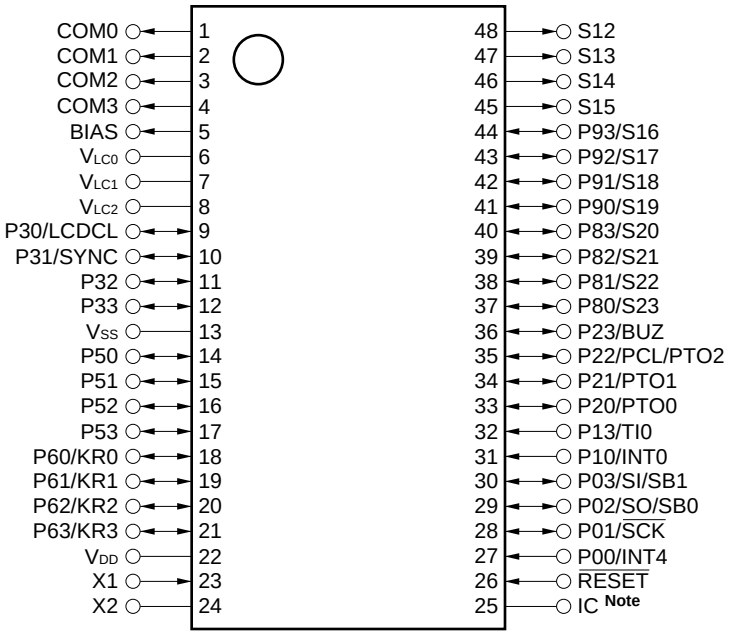
## Function Outline

| Parameter | | | Function |
|---|---|---|---|
| Instruction execution time | | | • 0.95, 1.91, 3.81, 15.3 μs (@ 4.19-MHz operation with system clock)<br>• 0.67, 1.33, 2.67, 10.7 μs (@ 6.0-MHz operation with system clock) |
| Internal memory | ROM | | 4096 × 8 bits (μPD753204) |
| | | | 6144 × 8 bits (μPD753206) |
| | | | 8192 × 8 bits (μPD753208) |
| | RAM | | 512 × 4 bits |
| General-purpose register | | | • 4-bit operation: 8 × 4 banks<br>• 8-bit operation: 4 × 4 banks |
| Input/ output port | CMOS input | 6 | Connecting on-chip pull-up resistors can be specified by software: 5 |
| | CMOS input/output | 20 | Connecting on-chip pull-up resistors can be specified by software: 20<br>Also used for segment pins: 8 |
| | N-ch open-drain input/output | 4 | On-chip pull-up resistors can be specified by mask option<br>13-V withstand voltage |
| | Total | | 30 |
| LCD controller/driver | | | • Segment selection: 4/8/12 segments (can be changed to CMOS input/ output port in 4-time units; max. 8)<br>• Display mode selection: Static<br>1/2 duty (1/2 bias)<br>1/3 duty (1/2 bias)<br>1/3 duty (1/3 bias)<br>1/4 duty (1/3 bias) |
| | | | • On-chip split resistor for LCD drive can be specified by mask option |
| Timer | | | 5 channels<br>• 8-bit timer/event counter: 1 channel<br>• 8-bit timer counter: 2 channels (can be used as the 16-bit timer counter, carrier generator, and timer with gate)<br>• Basic interval timer/watchdog timer: 1 channel<br>• Watch timer: 1 channel |
| Serial interface | | | • 3-wire serial I/O mode ... MSB or LSB can be selected for transferring first bit<br>• 2-wire serial I/O mode<br>• SBI mode |
| Bit sequential buffer (BSB) | | | 16 bits |
| Clock output (PCL) | | | • Φ, 524, 262, 65.5 kHz (@ 4.19-MHz operation with system clock)<br>• Φ, 750, 375, 93.8 kHz (@ 6.0-MHz operation with system clock) |
| Buzzer output (BUZ) | | | • 2, 4, 32 kHz (@ 4.19-MHz operation with system clock)<br>• 2.93, 5.86, 46.9 kHz (@ 6.0-MHz with system clock) |
| Vectored interrupts | | | External: 2, Internal: 5 |
| Test input | | | External: 1, Internal: 1 |
| System clock oscillator | | | Ceramic or crystal oscillator for system clock oscillation |
| Standby function | | | STOP/HALT mode |
| Power supply voltage | | | $V_{DD}$ = 1.8 to 5.5 V |
| Package | | | 48-pin plastic shrink SOP (375 mils, 0.65-mm pitch) |

CONTENTS

## 1. PIN CONFIGURATION (TOP VIEW)

- **48-pin plastic shrink SOP (375 mils, 0.65-mm pitch)**
  **μPD753204GT-×××, μPD753206GT-×××,**
  **μPD753208GT-×××**

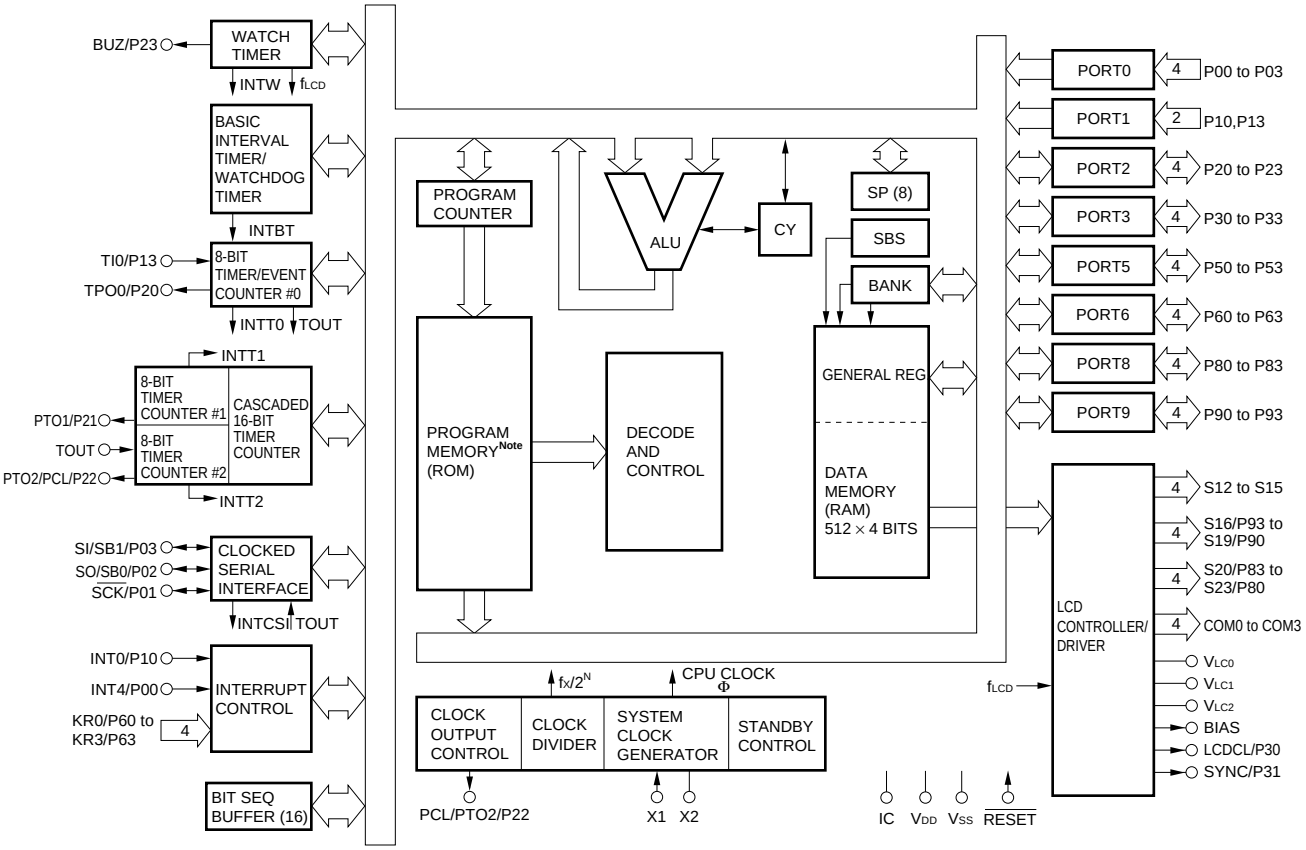



**Note** Connect IC (Internally Connected) pin directly to $V_{DD}$.

### Pin Identification

| | |
|---|---|
| P00 to P03 | : Port0 |
| P10, P13 | : Port1 |
| P20 to P23 | : Port2 |
| P30 to P33 | : Port3 |
| P50 to P53 | : Port5 |
| P60 to P63 | : Port6 |
| P80 to P83 | : Port8 |
| P90 to P93 | : Port9 |
| KR0 to KR3 | : Key Return 0 to 3 |
| COM0 to COM3 | : Common Output 0 to 3 |
| $\overline{SCK}$ | : Serial Clock |
| SI | : Serial Input |
| SO | : Serial Output |
| SB0, SB1 | : Serial Data Bus 0, 1 |
| S12 to S23 | : Segment Output 12 to 23 |
| $V_{LC0}$ to $V_{LC2}$ | : LCD Power Supply 0 to 2 |
| BIAS | : LCD Power Supply Bias Control |
| LCDCL | : LCD Clock |
| SYNC | : LCD Synchronization |
| TI0 | : Timer Input 0 |
| PTO0 to PTO2 | : Programmable Timer Output 0 to 2 |
| BUZ | : Buzzer Clock |
| PCL | : Programmable Clock |
| INT0, INT4 | : External Vectored Interrupt 0, 4 |
| X1, X2 | : System Clock Oscillation 1, 2 |
| $\overline{RESET}$ | : Reset |
| IC | : Internally Connected |
| $V_{DD}$ | : Positive Power Supply |
| $V_{SS}$ | : Ground |

## 2. BLOCK DIAGRAM




**Note** The ROM capacity depends on the product.

## 3. PIN FUNCTION

### 3.1 Port Pins (1/2)

| Pin Name | Input/Output | Alternate Function | Function | 8-bit I/O | After Reset | I/O Circuit TYPE Note 1 |
|---|---|---|---|---|---|---|
| P00 | Input | INT4 | 4-bit input port (PORT0). For P01 to P03, on-chip pull-up resistors can be specified by software in 3-bit units. | No | Input | (B) |
| P01 | Input/Output | $\overline{SCK}$ | | | | (F)-A |
| P02 | Input/Output | SO/SB0 | | | | (F)-B |
| P03 | Input/Output | SI/SB1 | | | | (M)-C |
| P10 | Input | INT0 | Input port in 1 bit unit (PORT1). On-chip pull-up resistors can be specified by software in 2-bit units. Noise elimination circuit can be specified with P10/INT0. | No | Input | (B)-C |
| P13 | | TI0 | | | | |
| P20 | Input/Output | PTO0 | 4-bit input/output port (PORT2). On-chip pull-up resistors can be specified by software in 4-bit units. | No | Input | E-B |
| P21 | | PTO1 | | | | |
| P22 | | PCL/PTO2 | | | | |
| P23 | | BUZ | | | | |
| P30 | Input/Output | LCDCL | Programmable 4-bit input/output port (PORT3). This port can be specified input/output bit-wise. On-chip pull-up resistor can be specified by software in 4-bit units. | No | Input | E-B |
| P31 | | SYNC | | | | |
| P32 | | – | | | | |
| P33 | | – | | | | |
| P50 to P53 Note 2 | Input/Output | – | N-ch open-drain 4-bit input/output port (PORT5). A pull-up resistor can be contained bit-wise (mask option). Withstand voltage is 13 V in open-drain mode. | No | High level (when pull-up resistors are provided) or high-impedance | M-D |

**Notes 1.** Characters in parentheses indicate the Schmitt-trigger input.

**2.** If on-chip pull-up resistors are not specified by mask option (when used as N-ch open-drain input port), low level input leakage current increases when input or bit manipulation instruction is executed.

### 3.1 Port Pins (2/2)

| Pin Name | Input/Output | Alternate Function | Function | 8-bit I/O | After Reset | I/O Circuit TYPE Note 1 |
|---|---|---|---|---|---|---|
| P60 | Input/Output | KR0 | Programmable 4-bit input/output port (PORT6). This port can be specified for input/output bit-wise. On-chip pull-up resistors can be specified by software in 4-bit units. | No | Input | (F)-A |
| P61 | | KR1 | | | | |
| P62 | | KR2 | | | | |
| P63 | | KR3 | | | | |
| P80 | Input/Output | S23 | 4-bit input/output port (PORT8). On-chip pull-up resistors can be specified by software in 4-bit units. Note 2 | Yes | Input | H |
| P81 | | S22 | | | | |
| P82 | | S21 | | | | |
| P83 | | S20 | | | | |
| P90 | Input/Output | S19 | 4-bit input/output port (PORT9). On-chip pull-up resistors can be specified by software in 4-bit units. Note 2 | | Input | H |
| P91 | | S18 | | | | |
| P92 | | S17 | | | | |
| P93 | | S16 | | | | |

**Notes 1.** Characters in parentheses indicate the Schmitt-trigger input.

**2.** Do not connect on-chip pull-up resistors specified by software when using as segment signal output pins.

### 3.2 Non-Port Pins (1/2)

| Pin Name | Input/Output | Alternate Function | Function | After Reset | I/O Circuit TYPE Note 1 |
|---|---|---|---|---|---|
| TI0 | Input | P13 | Inputs external event pulses to the timer/event counter. | Input | (B)-C |
| PTO0 | Output | P20 | Timer/event counter output | Input | E-B |
| PTO1 | | P21 | Timer counter output | | |
| PTO2 | | P22/PCL | | | |
| PCL | | P22/PTO2 | Clock output | | |
| BUZ | | P23 | Optional frequency output (for buzzer output or system clock trimming) | | |
| $\overline{SCK}$ | Input/Output | P01 | Serial clock input/output | Input | (F)-A |
| SO/SB0 | | P02 | Serial data output<br>Serial data bus input/output | | (F)-B |
| SI/SB1 | | P03 | Serial data input<br>Serial data bus input/output | | (M)-C |
| INT4 | Input | P00 | Edge detection vectored interrupt input (both rising edge and falling edge detection) | Input | (B) |
| INT0 | Input | P10 | Edge detection vectored interrupt input (detection edge can be selected). Noise elimination circuit can be specified. / With clock elimination circuit/asynchronous selectable | Input | (B)-C |
| KR0 to KR3 | Input/Output | P60 to P63 | Falling edge detection testable input | Input | (F)-A |
| S12 to S15 | Output | – | Segment signal output | **Note 2** | G-A |
| S16 to S19 | Output | P93 to P90 | Segment signal output | Input | H |
| S20 to S23 | Output | P83 to P80 | Segment signal output | Input | H |
| COM0 to COM3 | Output | – | Common signal output | **Note 2** | G-B |
| $V_{LC0}$ to $V_{LC2}$ | – | – | LCD drive power<br>On-chip split resistor is enable (mask option). | – | – |
| BIAS | Output | – | Output for external split resistor disconnect | **Note 3** | – |
| LCDCL Note 4 | Input/Output | P30 | Clock output for externally expanded driver | Input | E-B |
| SYNC Note 4 | Input/Output | P31 | Clock output for externally expanded driver sync | Input | E-B |

**Notes 1.** Characters in parentheses indicate the Schmitt trigger input.

**2.** Each display output selects the following VLCX as input source.
S12 to S15: $V_{LC1}$, COM0 to COM2: $V_{LC2}$, COM3: $V_{LC0}$.

**3.** When a split resistor is contained ..... Low level
When no split resistor is contained .....High-impedance

**4.** These pins are provided for future system expansion.
At present, these pins are used only as pins P30 and P31.

### 3.2 Non-Port Pins (2/2)

| Pin Name | Input/Output | Alternate Function | Function | After Reset | I/O Circuit TYPE Note 1 |
|---|---|---|---|---|---|
| X1 | Input | – | Crystal/ceramic connection pin for the system clock oscillator. When inputting the external clock, input the external clock to pin X1, and the reverse phase of the external clock to pin X2. | – | – |
| X2 | – | | | | |
| $\overline{\text{RESET}}$ | Input | – | System reset input (low-level active) | – | (B) |
| IC | – | – | Internally connected. Connect directly to $V_{DD}$. | – | – |
| $V_{DD}$ | – | – | Positive power supply | – | – |
| $V_{SS}$ | – | – | Ground potential | – | – |

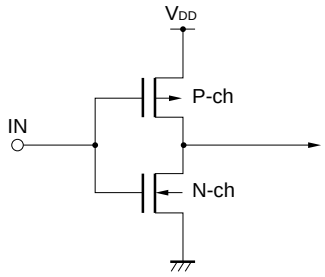
**Note** Characters in parentheses indicate the Schmitt-trigger input.

### 3.3 Pin Input/Output Circuits

The μPD753208 pin input/output circuits are shown schematically.

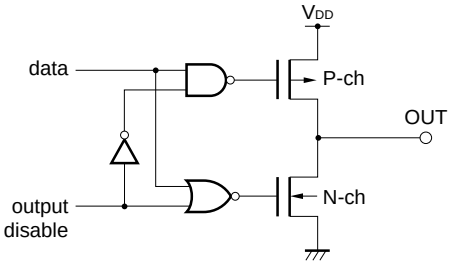
(1/2)

TYPE A



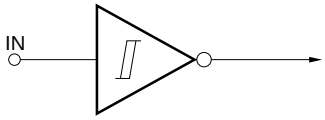

CMOS specification input buffer.

TYPE D



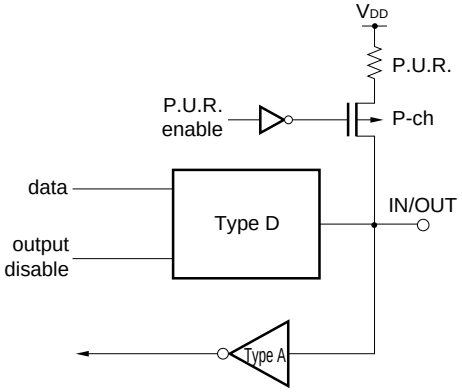

Push-pull output that can be placed in output high-impedance (both P-ch, N-ch off).

TYPE B



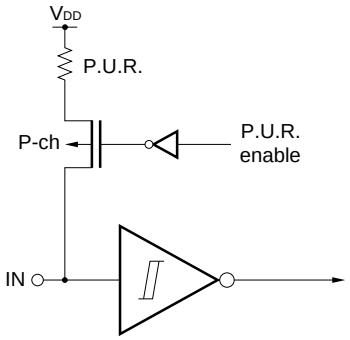

Schmitt trigger input having hysteresis characteristic.

TYPE E-B



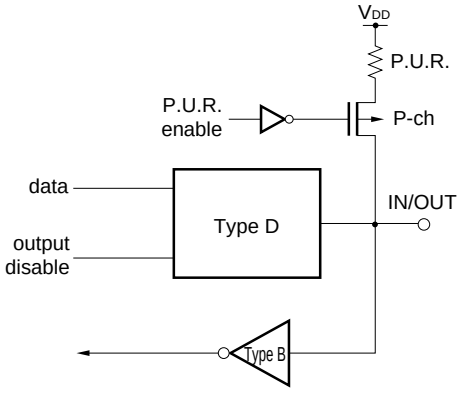

P.U.R. : Pull-Up Resistor

TYPE B-C




P.U.R. : Pull-Up Resistor

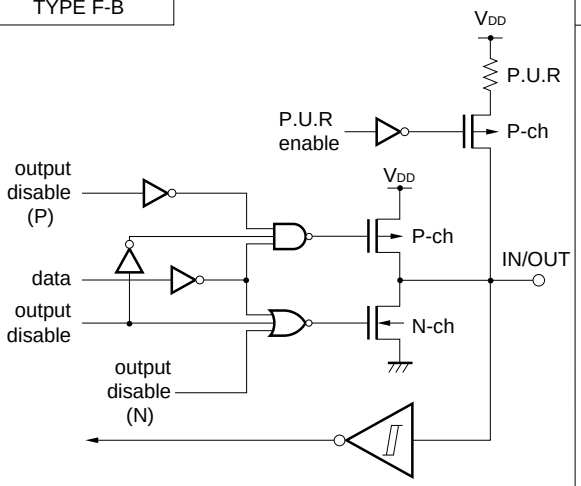
TYPE F-A




P.U.R. : Pull-Up Resistor

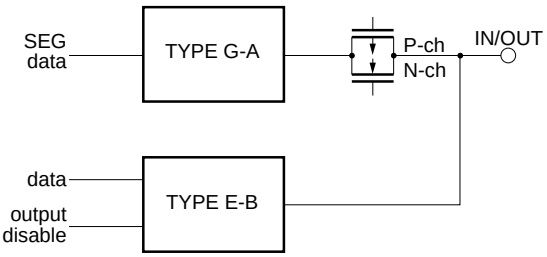
(2/2)

TYPE F-B

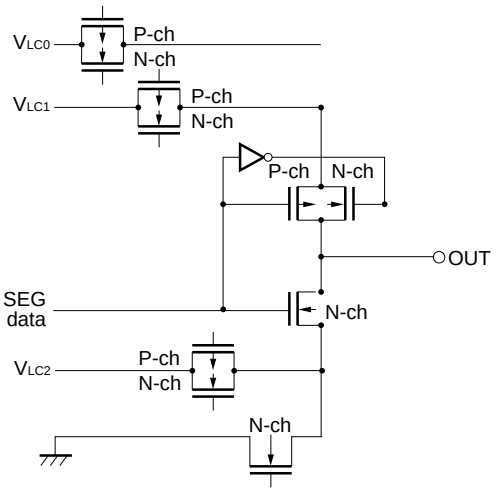



P.U.R : Pull-Up Resistor

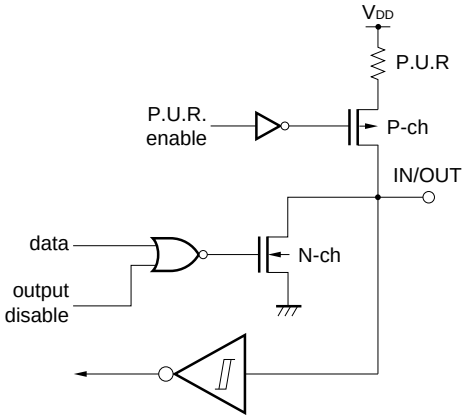
TYPE H




TYPE G-A

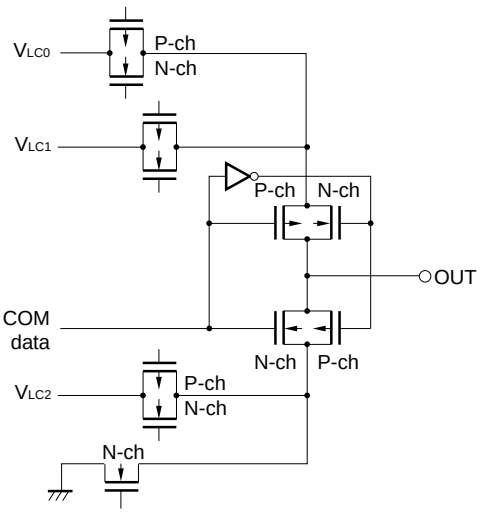



TYPE M-C

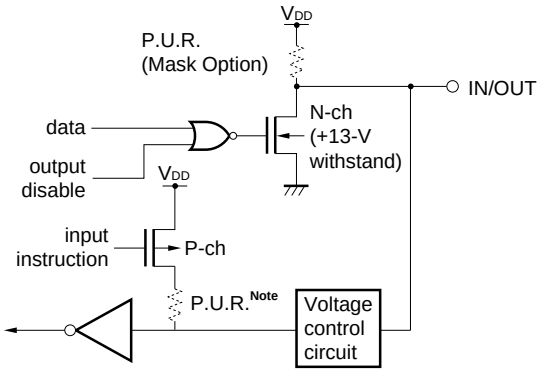



P.U.R : Pull-Up Resistor

TYPE G-B




TYPE M-D




P.U.R. : Pull-Up Resistor

**Note** Pull-up resistor that only operates upon the execution of an input instruction when the pull-up resistor is not connected via the mask option (it is available during low-voltage).

### 3.4 Recommended Connections for Unused Pins

★ **Table 3-1. List of Recommended Connections for Unused Pins**

| Pin | Recommended Connection |
|---|---|
| P00/INT4 | Connect to $V_{SS}$ or $V_{DD}$ |
| P01/$\overline{SCK}$ | Connect individually to $V_{SS}$ or $V_{DD}$ via a resistor |
| P02/SO/SB0 | |
| P03/SI/SB1 | Connect to $V_{SS}$ |
| P10/INT0 | Connect to $V_{SS}$ or $V_{DD}$ |
| P13/TI0 | |
| P20/PTO0 | Input state: Connect individually to $V_{SS}$ or $V_{DD}$ via a resistor<br>Output state: No connection |
| P21/PTO1 | |
| P22/PCL/PTO2 | |
| P23/BUZ | |
| P30/LCDCL | |
| P31/SYNC | |
| P32 | |
| P33 | |
| P50 to P53 | Input state : Connect to $V_{SS}$<br>Output state : Connect to $V_{SS}$ (Do not connect pull-up resistor in the mask option) |
| P60/KR0 to P63/KR3 | Input state : Connect individually to $V_{SS}$ or $V_{DD}$ via a resistor<br>Output state : No connection |
| S0 to S15 | No connection |
| COM0 to COM3 | |
| S16/P93 to S19/P90 | Input state: Connect individually to $V_{SS}$ or $V_{DD}$ via a resistor<br>Output state: No connection |
| S20/P83 to S23/P80 | |
| $V_{LC0}$ to $V_{LC2}$ | Connect to $V_{SS}$ |
| BIAS | Only if all of $V_{LC0}$ to $V_{LC2}$ are unused, connect to $V_{SS}$.<br>In other cases, no connection. |
| IC | Connect to $V_{DD}$ directly |

# 4 SWITCHING FUNCTION BETWEEN Mk I MODE AND Mk II MODE

## 4.1 Difference Between Mk I and Mk II Modes

The CPU of the μPD753208 has the following two modes: Mk I and Mk II, either of which can be selected. The mode can be switched by bit 3 of the Stack Bank Select register (SBS).

- Mk I mode: Upward compatible with the μPD75308B. Can be used in the 75XL CPU with a ROM capacity of up to 16 Kbytes.
- Mk II mode: Incompatible with μPD75308B. Can be used in all the 75XL CPU including those products whose ROM capacity is more than 16 Kbytes.

**Table 4-1. Differences between Mk I Mode and Mk II Mode**

| | Mk I mode | Mk II mode |
|---|---|---|
| Number of stack bytes for subroutine instructions | 2 bytes | 3 bytes |
| BRA ! addr1 instruction<br>CALLA ! addr1 instruction | Not available | Available |
| CALL ! addr instruction | 3 machine cycles | 4 machine cycles |
| CALLF ! faddr instruction | 2 machine cycles | 3 machine cycles |

★ **Caution The MkII mode supports a program area exceeding 16 Kbytes for the 75X and 75XL Series. Software compatibility with products whose program memory exceeds 16 Kbytes can be raised by using this mode.**

**When the MkII mode is selected, the number of stack bytes increases by one byte per stack during subroutine call instruction execution compared with the MkI mode. When the !faddr instruction is used, the length of each machine cycle increases by 1 machine cycle. Therefore, if RAM efficiency or processing speed is emphasized over software compatibility, use of the MkI mode is recommended.**

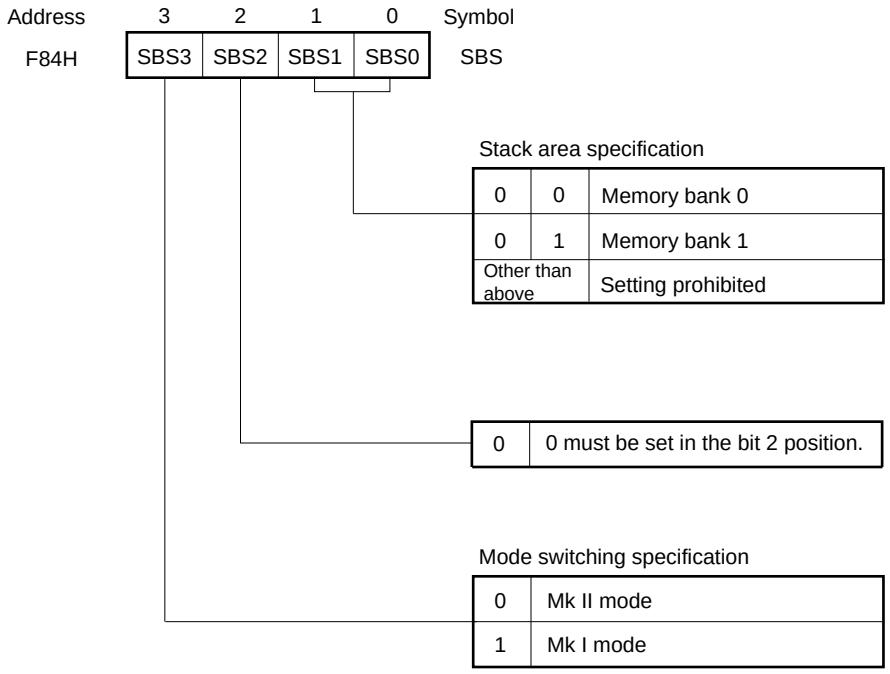
### 4.2 Setting Method of Stack Bank Select Register (SBS)

Switching between the Mk I mode and Mk II mode can be done by the SBS. Figure 4-1 shows the format.

The SBS is set by a 4-bit memory manipulation instruction. When using the Mk I mode, the SBS must be initialized to 100×B[Note] at the beginning of a program. When using the Mk II mode, it must be initialized to 000×B[Note].

**Note** The desired numbers must be set in the × positions.

**Figure 4-1. Stack Bank Select Register Format**




**Caution Since SBS. 3 is set to "1" after a $\overline{\text{RESET}}$ signal is generated, the CPU operates in the Mk I mode. When executing an instruction in the Mk II mode, set SBS. 3 to "0" to select the Mk II mode.**

## 5. MEMORY CONFIGURATION

- **Program Memory (ROM) .... 4096 × 8 bits (μPD753204)**
  **.... 6144 × 8 bits (μPD753206)**
  **.... 8192 × 8 bits (μPD753208)**

  – Addresses 0000H and 0001H
  Vector table wherein the program start address and the values set for the RBE and MBE at the time a $\overline{\text{RESET}}$ signal is generated are written. Reset and start are possible at an arbitrary address.

  – Addresses 0002H to 000DH
  Vector table wherein the program start address and values set for the RBE and MBE by the vectored interrupts are written. Interrupt execution can be started at an arbitrary address.

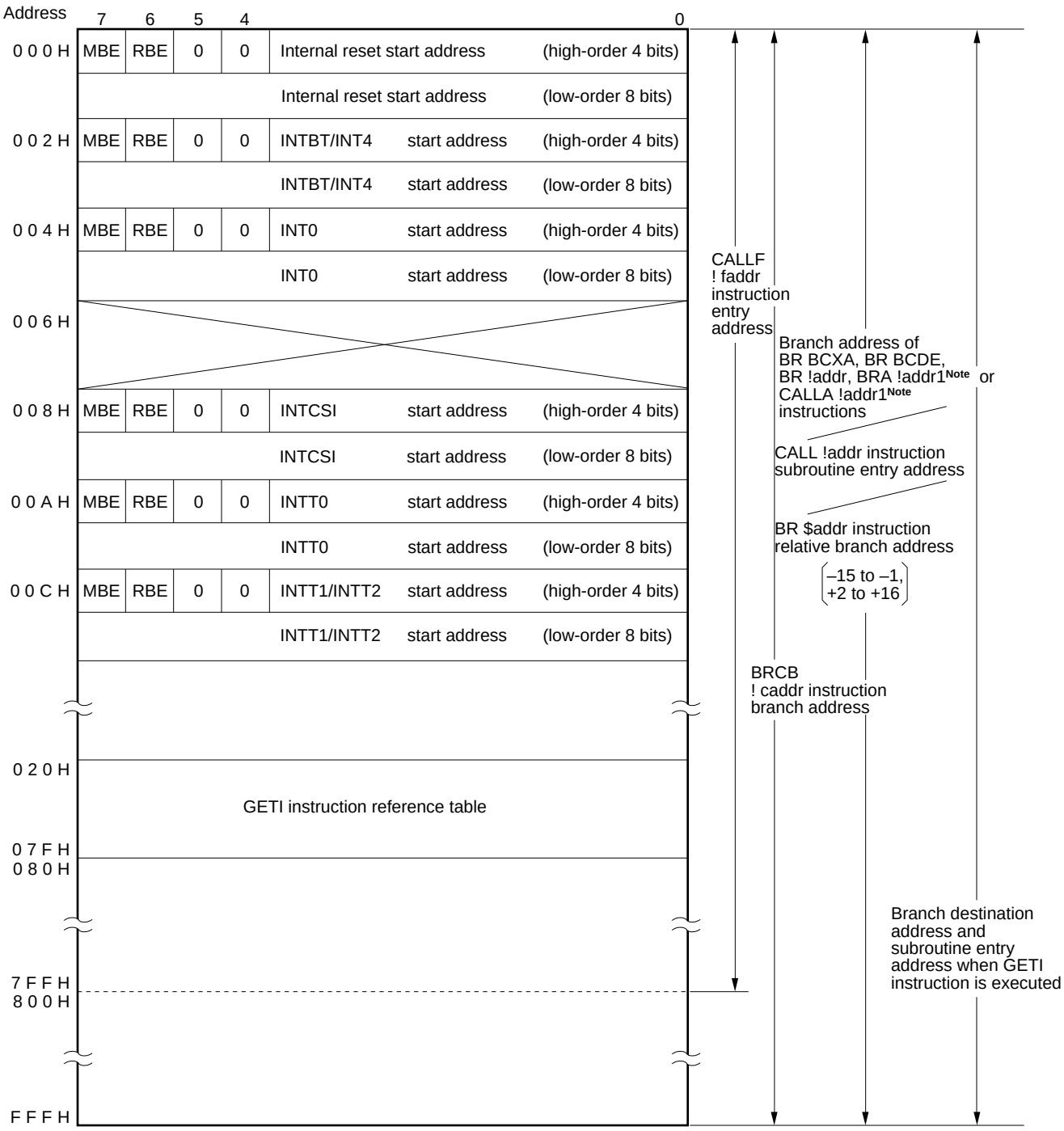
  – Addresses 0020H to 007FH
  Table area referenced by the GETI instruction [Note].

**Note** The GETI instruction realizes a 1-byte instruction on behalf of an arbitrary 2-byte instruction, 3-byte instruction, or two 1-byte instructions. It is used to decrease the program steps.

- **Data Memory (RAM)**
  – Data area ... 512 words × 4 bits (000H to 1FFH)
  – Peripheral hardware area ... 128 words × 4 bits (F80H to FFFH)

**Figure 5-1. Program Memory Map (1/3)**

**(a) μPD753204**

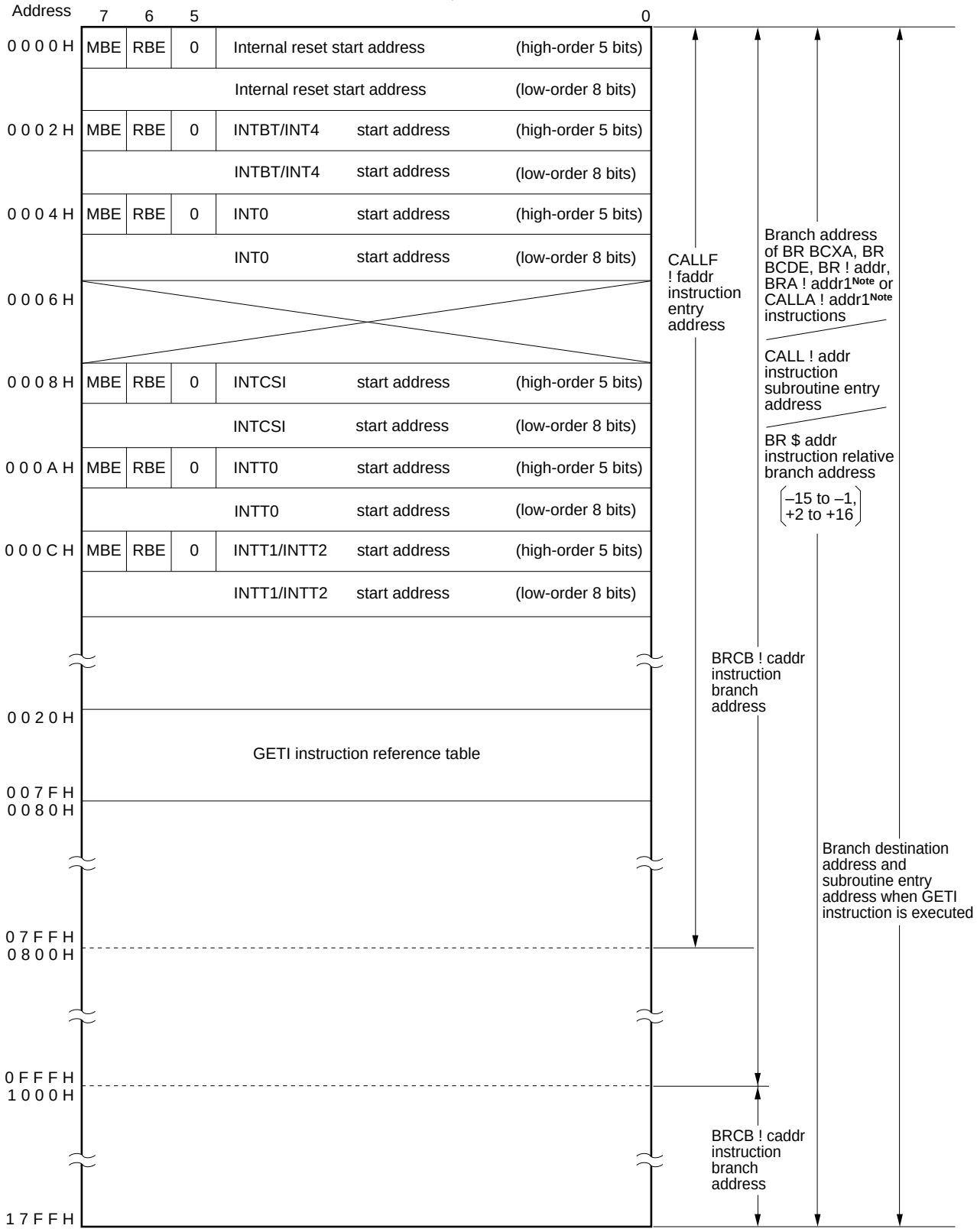



**Note** Can be used only in the Mk II mode.

**Remark** In addition to the above, a branch can be taken to the address indicated by changing only the low-order eight bits of PC by executing the BR PCDE or BR PCXA instruction.

**Figure 5-1. Program Memory Map (2/3)**

**(b) μPD753206**

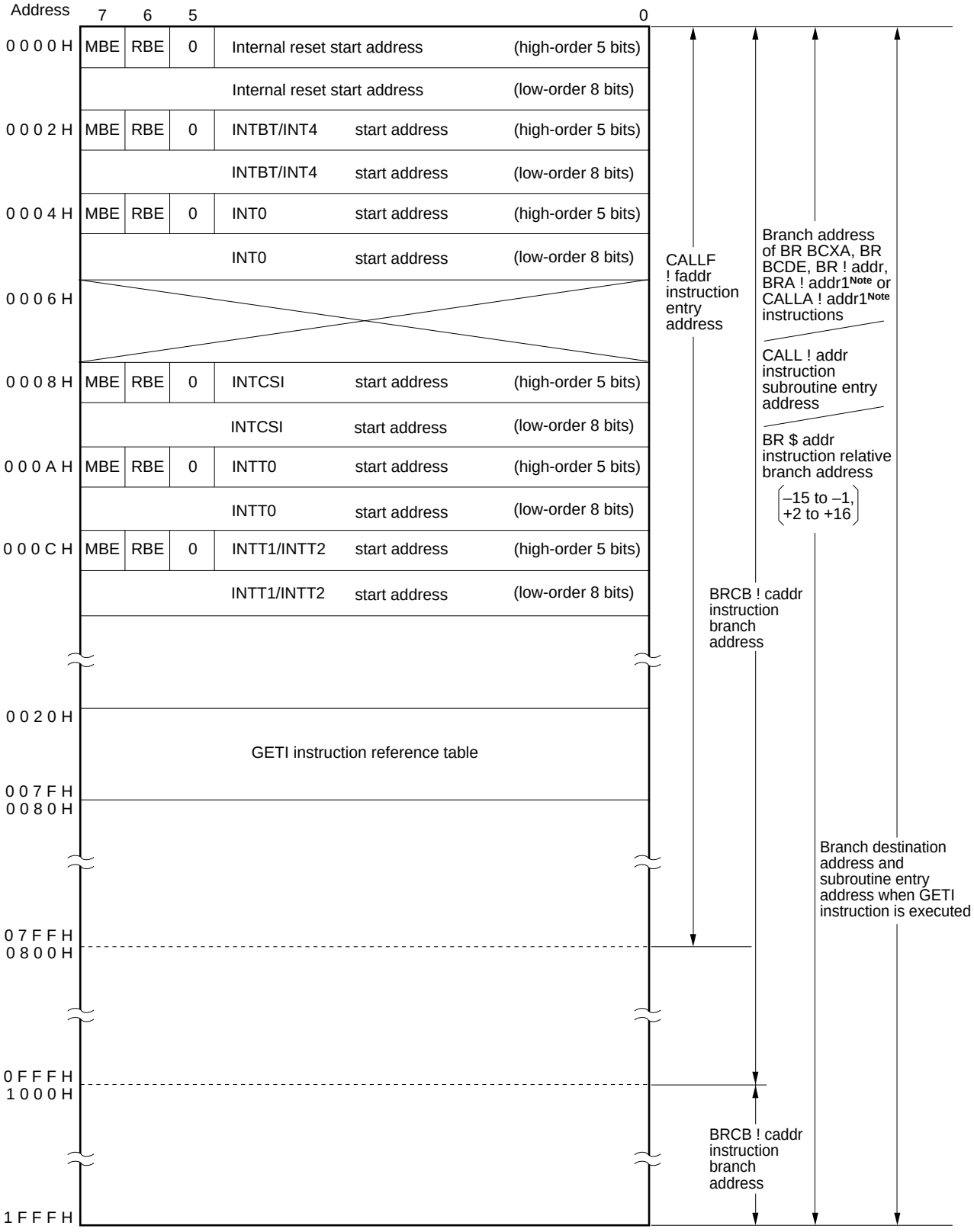



**Note** Can be used only in the Mk II mode.

**Remark** In addition to the above, a branch can be taken to the address indicated by changing only the low-order eight bits of PC by executing the BR PCDE or BR PCXA instruction.

**Figure 5-1. Program Memory Map (3/3)**

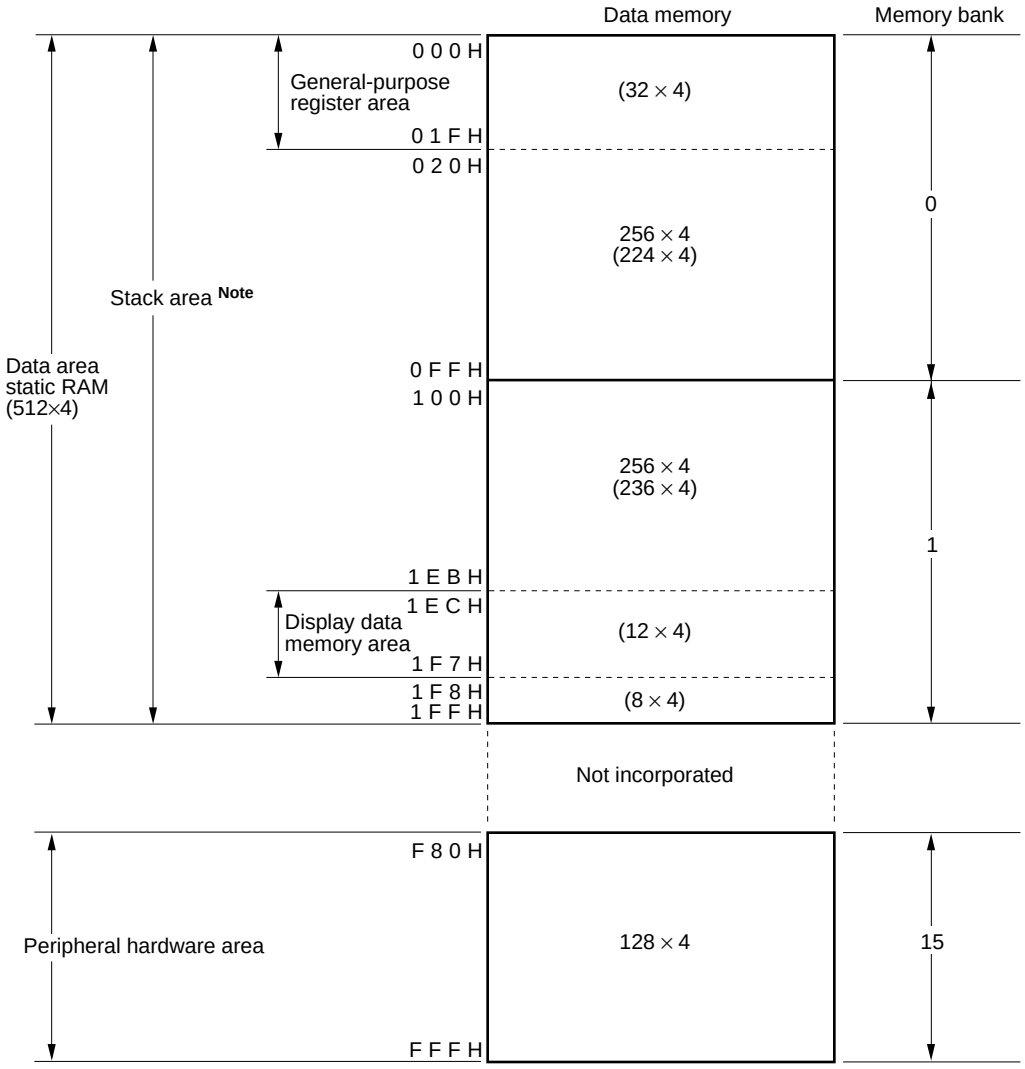
**(c) μPD753208**




**Note** Can be used only in the Mk II mode.

**Remark** In addition to the above, a branch can be taken to the address indicated by changing only the low-order eight bits of PC by executing the BR PCDE or BR PCXA instruction.

**Figure 5-2. Data Memory Map**




**Note** As a stack area, either memory bank 0 or 1 can be selected.

# 6. PERIPHERAL HARDWARE FUNCTION

## 6.1 Digital I/O Port

There are three kinds of I/O ports.

- CMOS input ports (Ports 0, 1) : 6
- CMOS input/output ports (Ports 2, 3, 6, 8, 9) : 20
- N-ch open-drain input/output ports (Port 5) : 4

Total 30

**Table 6-1. Types and Features of Digital Ports**

| Port | Function | Operation and features | | Remarks |
|---|---|---|---|---|
| PORT0 | 4-bit input | The alternate function pins have an output function with operation mode when using the serial interface function. | | Also used for the INT4, $\overline{SCK}$, SO/SB0, and SI/SB1 pins. |
| PORT1 | 1-bit input | 2-bit input dedicated port | | Also used for the INT0 and TI0. |
| PORT2 | 4-bit I/O | Can be set to input mode or output mode in 4-bit units. | | Also used for the PTO0 to PTO2, PCL, and BUZ pins. |
| PORT3 | | Can be set to input mode or output mode bit-wise. | | Also used for the LCDCL and SYNC pins. |
| PORT5 | 4-bit I/O (N-channel open-drain, 13-V withstand) | Can be set to input mode or output mode in 4-bit units. On-chip pull-up resistor can be specified by mask option bit-wise. | | — |
| PORT6 | 4-bit I/O | Can be set to input mode or output mode bit-wise. | | Also used for the KR0 to KR3 pins. |
| PORT8 | | Can be set to input mode or output mode in 4-bit units. | Ports 8 and 9 are paired and data can be input/output in 8-bit units. | Also used for the S20 to S23 pins. |
| PORT9 | | | | Also used for the S16 to S19 pins. |

### 6.2 Clock Generator

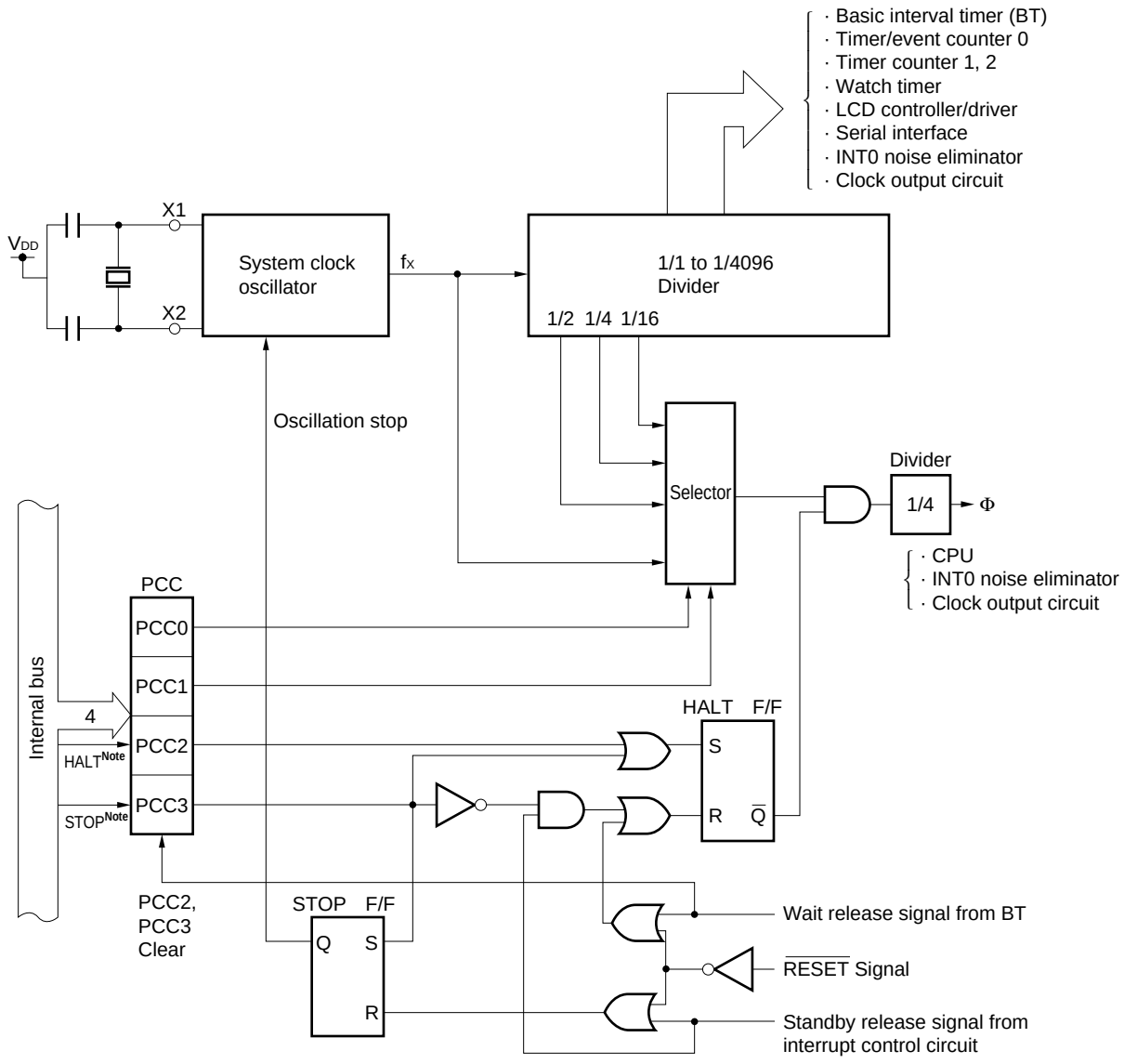
The clock generator provides the clock signals to the CPU and peripheral hardware and its configuration is shown in Figure 6-1.

The operation of the clock generator is determined by the Processor Clock Control Register (PCC).

The instruction execution time can also be changed.

- 0.95, 1.91, 3.81, 15.3 μs (system clock: @ 4.19-MHz operation)
- 0.67, 1.33, 2.67, 10.7 μs (system clock: @ 6.0-MHz operation)

**Figure 6-1. Clock Generator Block Diagram**




**Note** Instruction execution

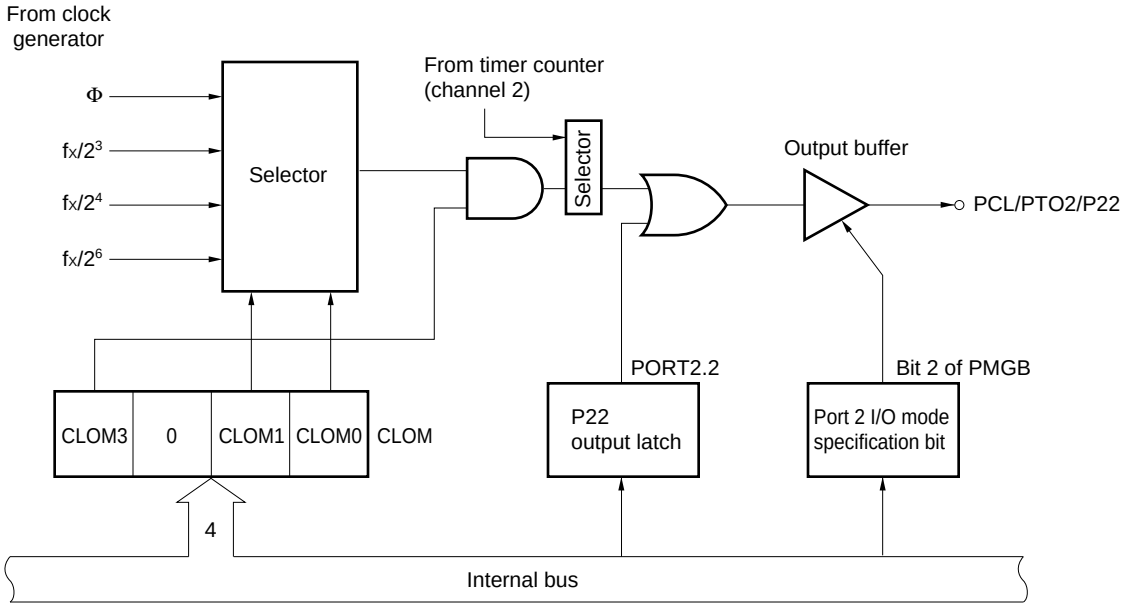
**Remarks** **1.** $f_X$ = System clock frequency
**2.** Φ = CPU clock
**3.** PCC: Processor Clock Control Register
**4.** One clock cycle ($t_{CY}$) of the CPU clock is equal to one machine cycle of the instruction.

### 6.3 Clock Output Circuit

The clock output circuit is provided to output the clock pulses from the PCL pin (also functions as P22 or PTO2) to the remote control wave outputs and peripheral LSIs.

- Clock Output (PCL) : Φ, 524, 262, 65.5 kHz (system clock: @ 4.19-MHz operation)
  Φ, 750, 375, 93.8 kHz (system clock: @ 6.0-MHz operation)

**Figure 6-2. Clock Output Circuit Block Diagram**



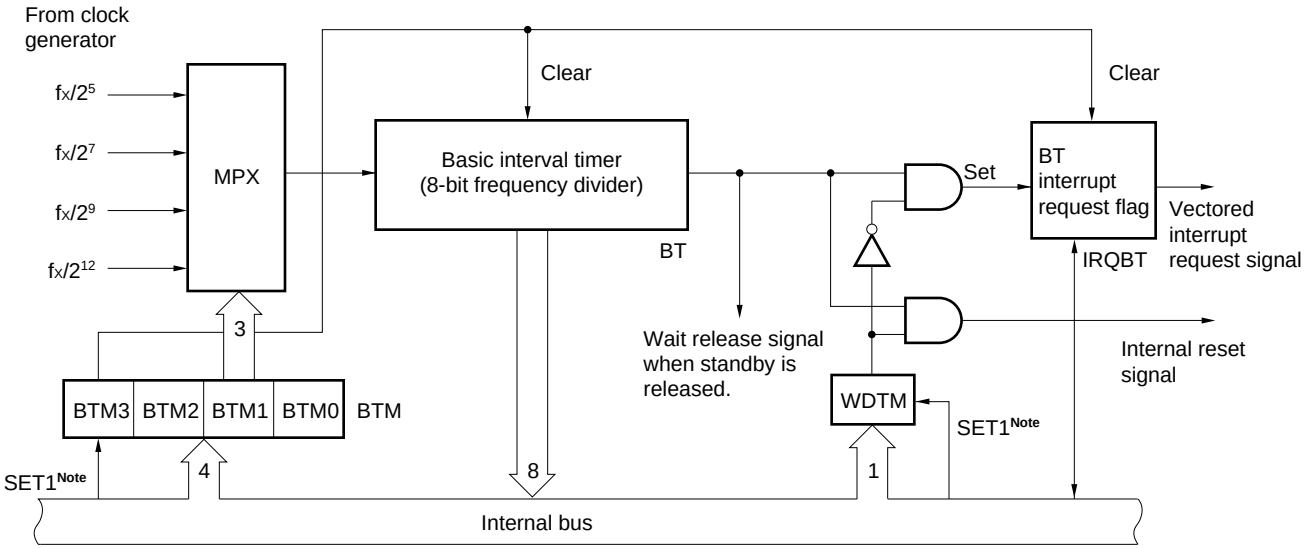

**Remark** Special care has been taken in designing the chip so that small-width pulses may not be output when switching clock output enable/disable.

### 6.4 Basic Interval Timer/Watchdog Timer

The basic interval timer/watchdog timer has the following functions.

- Interval timer operation to generate a reference time interrupt
- Watchdog timer operation to detect program runaway and reset the CPU
- Selects and counts the wait time when the standby mode is released
- Reads the contents of counting

**Figure 6-3. Basic Interval Timer/Watchdog Timer Block Diagram**



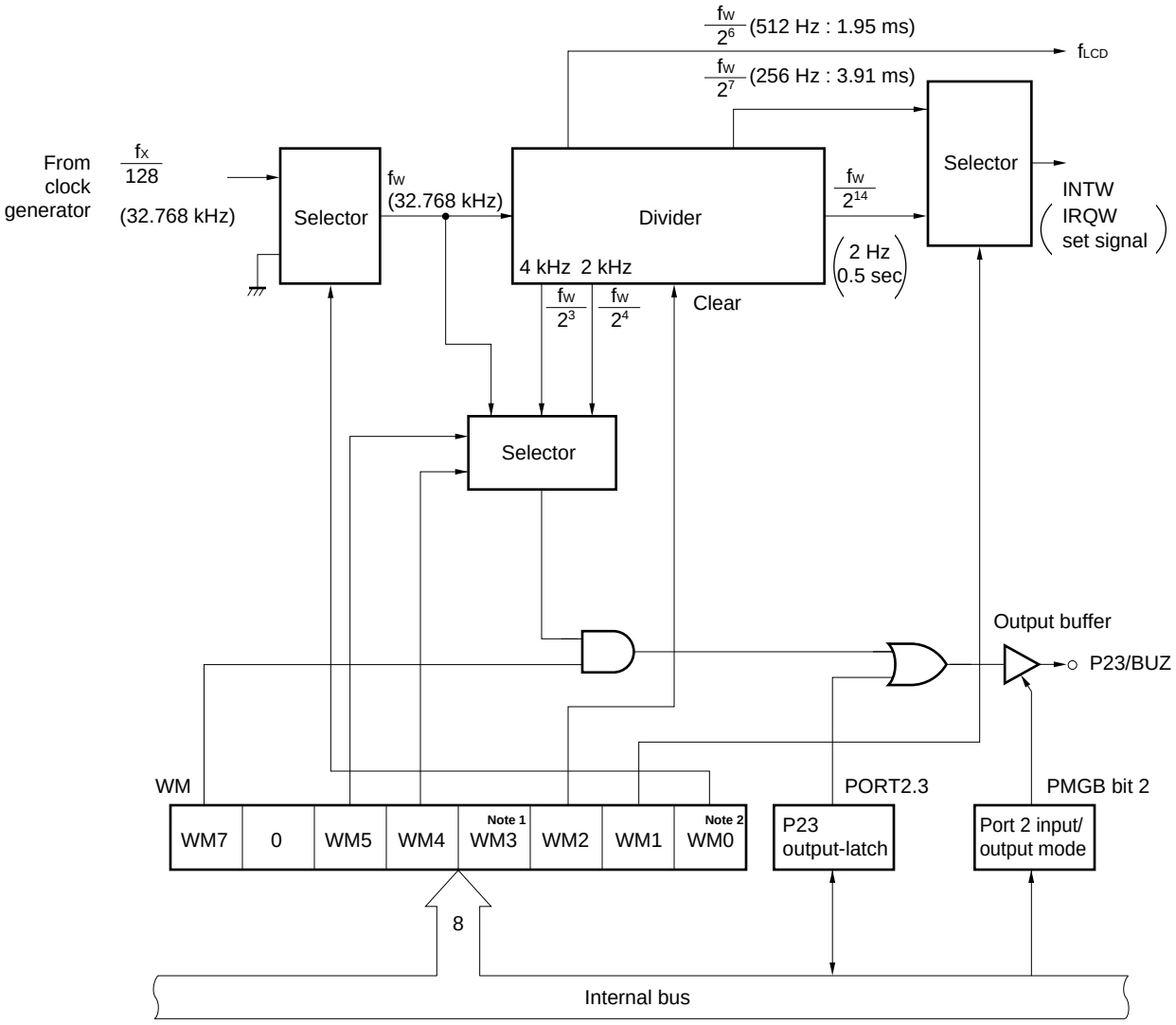

**Note** Instruction execution

### 6.5 Watch Timer

The μPD753208 has one watch timer channel, whose functions are as follows.

- Sets the test flag (IRQW) with 0.5 sec interval. The standby mode can be released by the IRQW.
- 0.5 sec interval can be created with the system clock (4.194304 MHz)
- Convenient for program debugging and checking as interval becomes 128 times longer (3.91 ms) with the fast feed mode.
- Outputs a frequency (2.048, 4.096, or 32.768 kHz) to the BUZ pin (P23), usable for buzzer and trimming of system clock frequencies.
- Clears the frequency divider to make the clock start with zero seconds.

**Figure 6-4. Watch Timer Block Diagram**




**Notes 1.** WM3 is undefined while reading data.

**2.** Be sure to set WM0 to 0.

**Remark** The values enclosed in parentheses are applied when $f_X$ = 4.194304 MHz.

### 6.6 Timer/Event Counter

The μPD753208 provides one channel for timer/event counters and two channels for timer counters. Figures 6-5 to 6-7 show the block diagrams. Timer/event counter functions are as follows.

- Programmable interval timer operation
- Square wave output of any frequency to the PTO0 pin (n = 0 to 2).
- Event counter operation (Channel 0 only)
- Divides the frequency of signal input via the TI0 pin to 1-nth of the original signal and outputs the divided frequency to the PTO0 pin (frequency divider operation).
- Supplies the shift clock to the serial interface circuit.
- Reads the counting status.

The timer/event counter operates in the following four modes as set by the mode register.

**Table 6-2. Operation Modes of Timer/Event Counter**

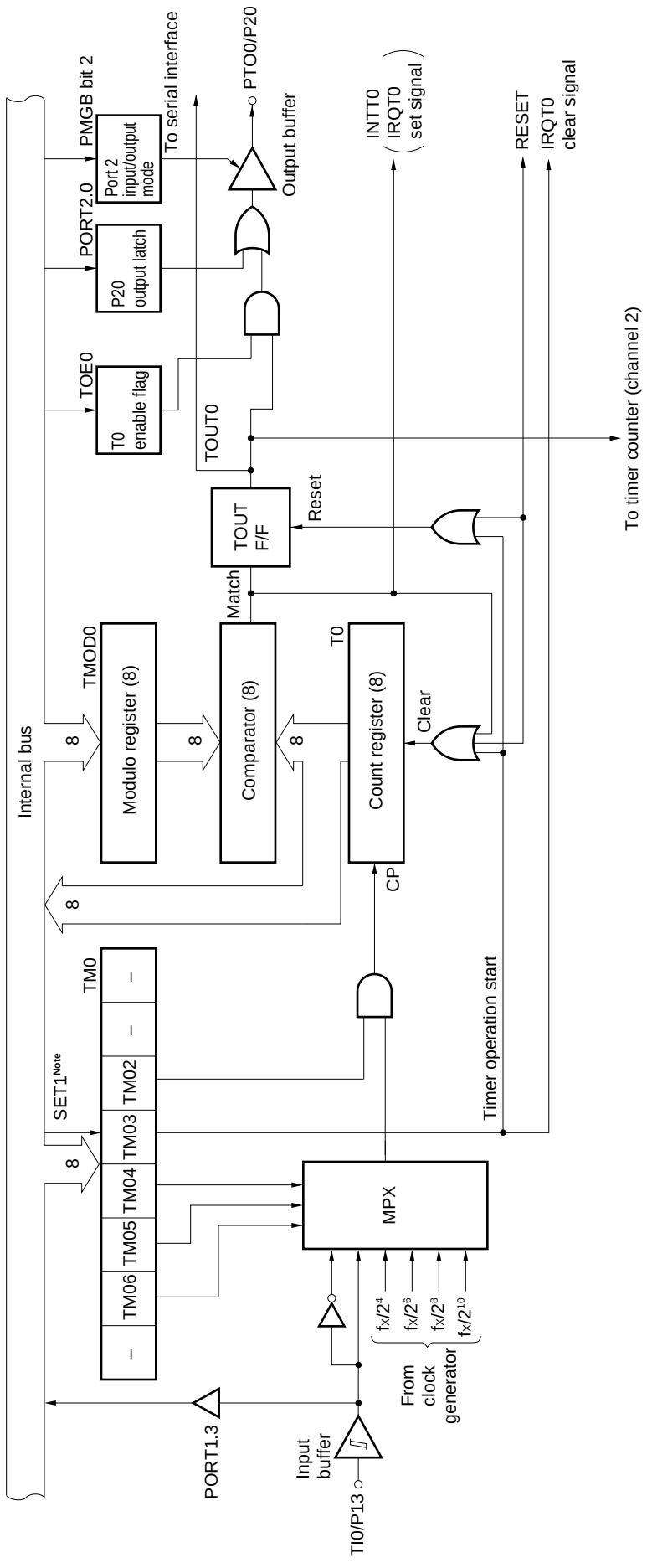
| Mode \ Channel | | Channel 0 | Channel 1 | Channel 2 |
|---|---|---|---|---|
| 8-bit timer/event counter mode Note 1 | | A | A | A |
| | Gate control function | N/A Note 2 | N/A | A |
| PWM pulse generator mode | | N/A | N/A | A |
| 16-bit timer counter mode | | N/A | A | |
| | Gate control function | N/A Note 2 | A | |
| Carrier generator mode | | N/A | A | |

**Notes 1.** Channel 0 only. 8-bit timer counter mode for channel 1 and channel 2

**2.** Used for gate control signal generation

**Remark** A: Available
N/A: Not available

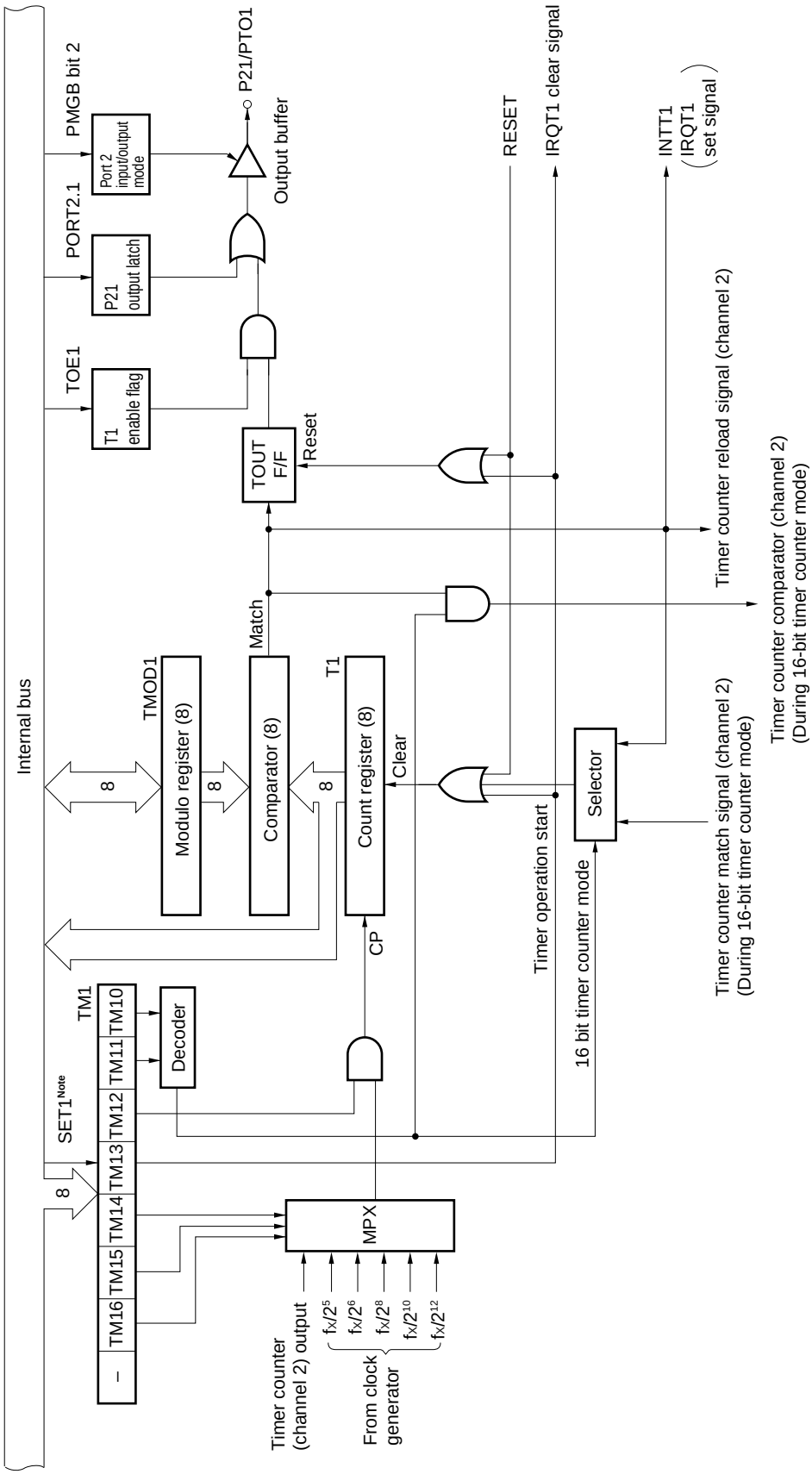
★**Figure 6-5. Timer/Event Counter Block Diagram (channel 0)**




**Note** Execution of instruction

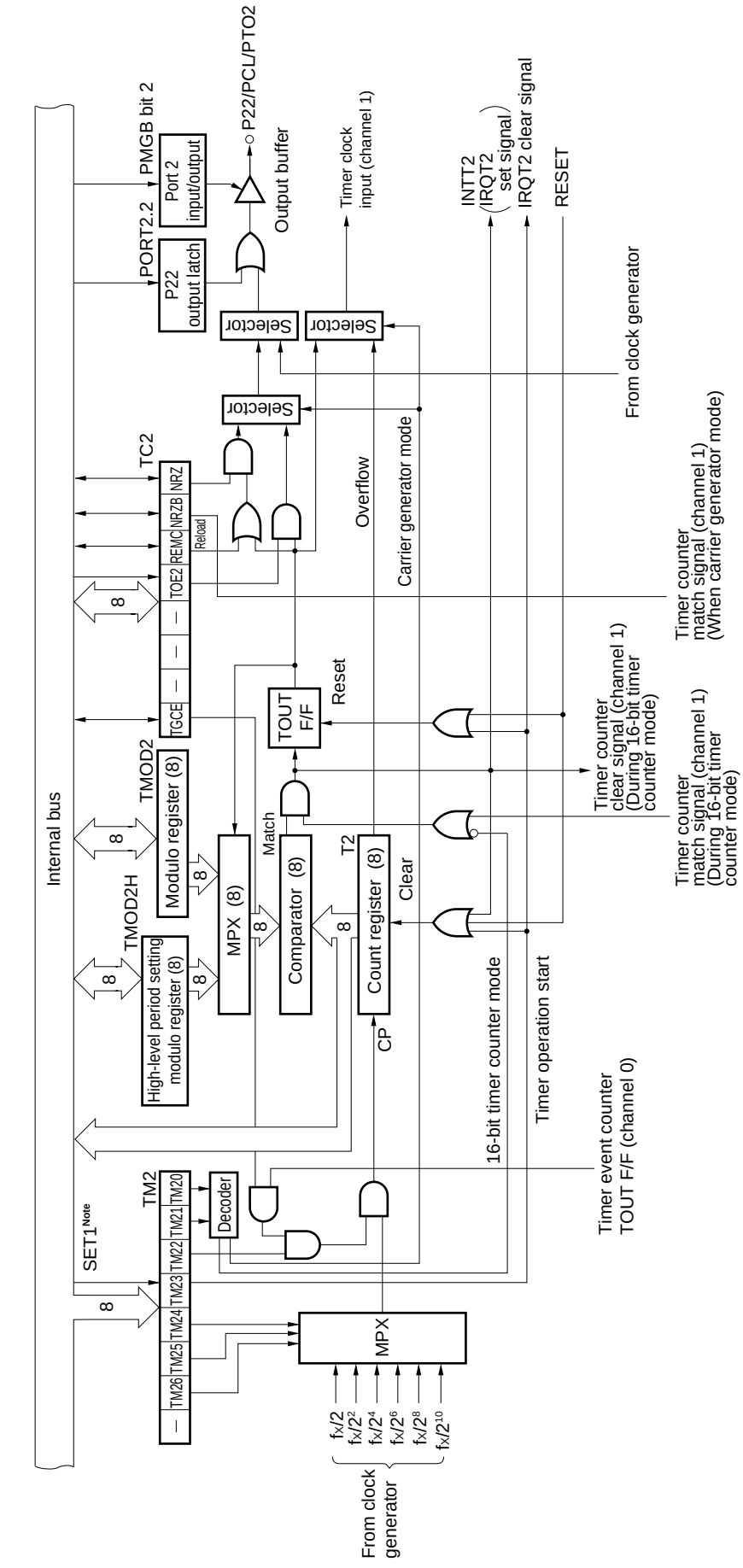
**Caution When data is set to TM0, always set bit 1 to 0.**

**Figure 6-6. Timer/Event Counter Block Diagram (channel 1)**




**Note** Execution of instruction

**Figure 6-7. Timer Counter Block Diagram (channel 2)**



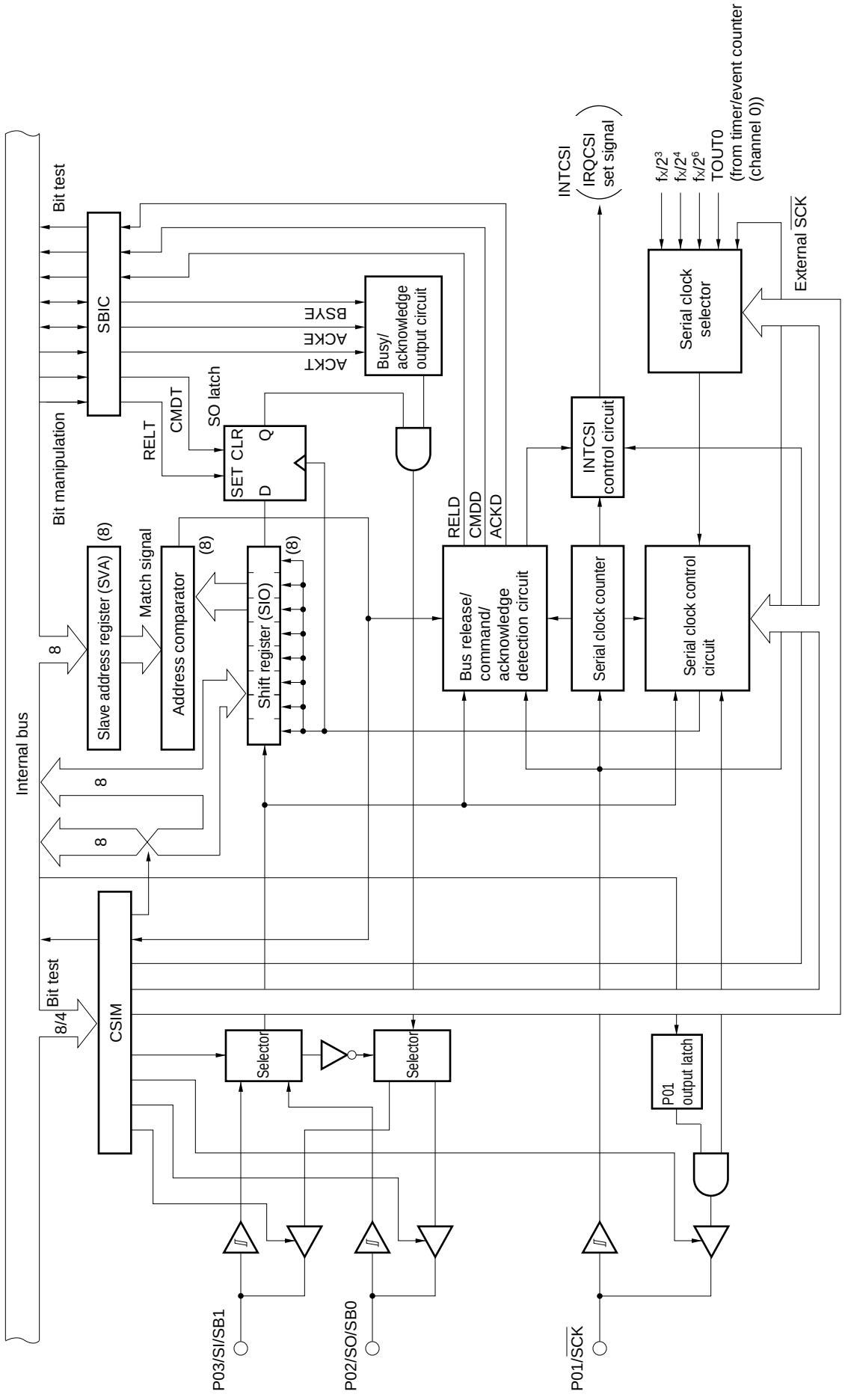

**Note** Execution of instruction

### 6.7 Serial Interface

The μPD753208 incorporates a clock-synchronous 8-bit serial interface and can be used in the following four modes.

- Operation stop mode
- 3-wire serial I/O mode
- 2-wire serial I/O mode
- SBI mode (serial bus interface mode)

**Figure 6-8. Serial Interface Block Diagram**



### 6.8 LCD Controller/Driver

The μPD753208 incorporates a display controller which generates segment and common signals according to the display data memory contents and incorporates segment and common drivers which can drive the panel directly.

The μPD753208 LCD controller/driver functions are as follows:

- Display data memory is read automatically by DMA operation and segment and common signals are generated.
- Display mode can be selected from among the following five:
  - <1> Static
  - <2> 1/2 duty (time multiplexing by 2), 1/2 bias
  - <3> 1/3 duty (time multiplexing by 3), 1/2 bias
  - <4> 1/3 duty (time multiplexing by 3), 1/3 bias
  - <5> 1/4 duty (time multiplexing by 4), 1/3 bias
- A frame frequency can be selected from among four in each display mode.
- A maximum of 12 segment signal output pins (S12 to S23) and four common signal output pins (COM0 to COM3).
- The segment signal output pins (S16 to S23) can be changed to the I/O ports (PORT8 and PORT9).
- Split-resistor can be incorporated to supply LCD drive power. (Mask option)
  - Various bias methods and LCD drive voltages can be applicable.
  - When display is off, current flowing through the split resistor is cut.
- Display data memory not used for display can be used for normal data memory.

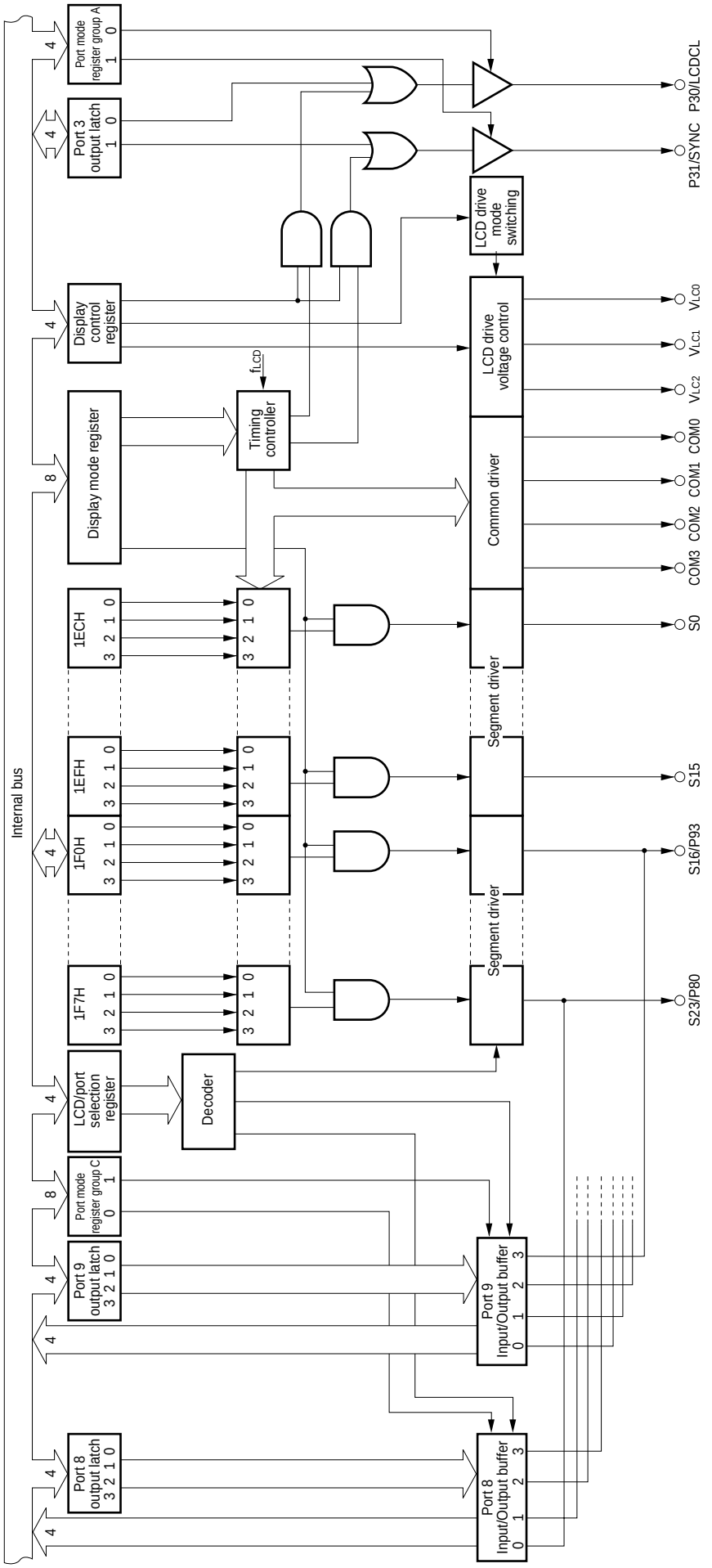
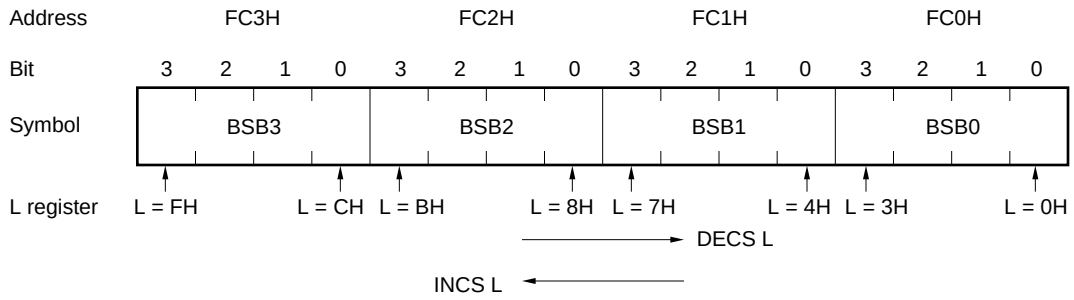



**Figure 6-9. LCD Controller/Driver Block Diagram**

### 6.9 Bit Sequential Buffer ..... 16 Bits

The bit sequential buffer (BSB) is a special data memory for bit manipulation and the bit manipulation can be easily performed by changing the address specification and bit specification in sequence, therefore it is useful when processing large data bit-wise.

**Figure 6-10. Bit Sequential Buffer Format**




**Remarks 1.** In pmem.@L addressing, the specified bit moves corresponding to the L register.

**2.** In pmem.@L addressing, the BSB can be manipulated regardless of MBE/MSB specification.

## 7. INTERRUPT FUNCTION AND TEST FUNCTION

There are seven interrupt sources and two test sources in the μPD753208.
The interrupt control circuit of the μPD753208 has the following functions.

**(1) Interrupt function**

- Vectored interrupt function for hardware control, enabling/disabling the interrupt acceptance by the interrupt enable flag (IE×××) and interrupt master enable flag (IME).
- Can set any interrupt start address.
- Multiple interrupts wherein the order of priority can be specified by the interrupt priority select register (IPS).
- Test function of interrupt request flag (IRQ×××). An interrupt generated can be checked by software.
- Release the standby mode. A release interrupt can be selected by the interrupt enable flag.

**(2) Test function**

- Test request flag (IRQ×××) generation can be checked by software.
- Release the standby mode. The test source to be released can be selected by the test enable flag.

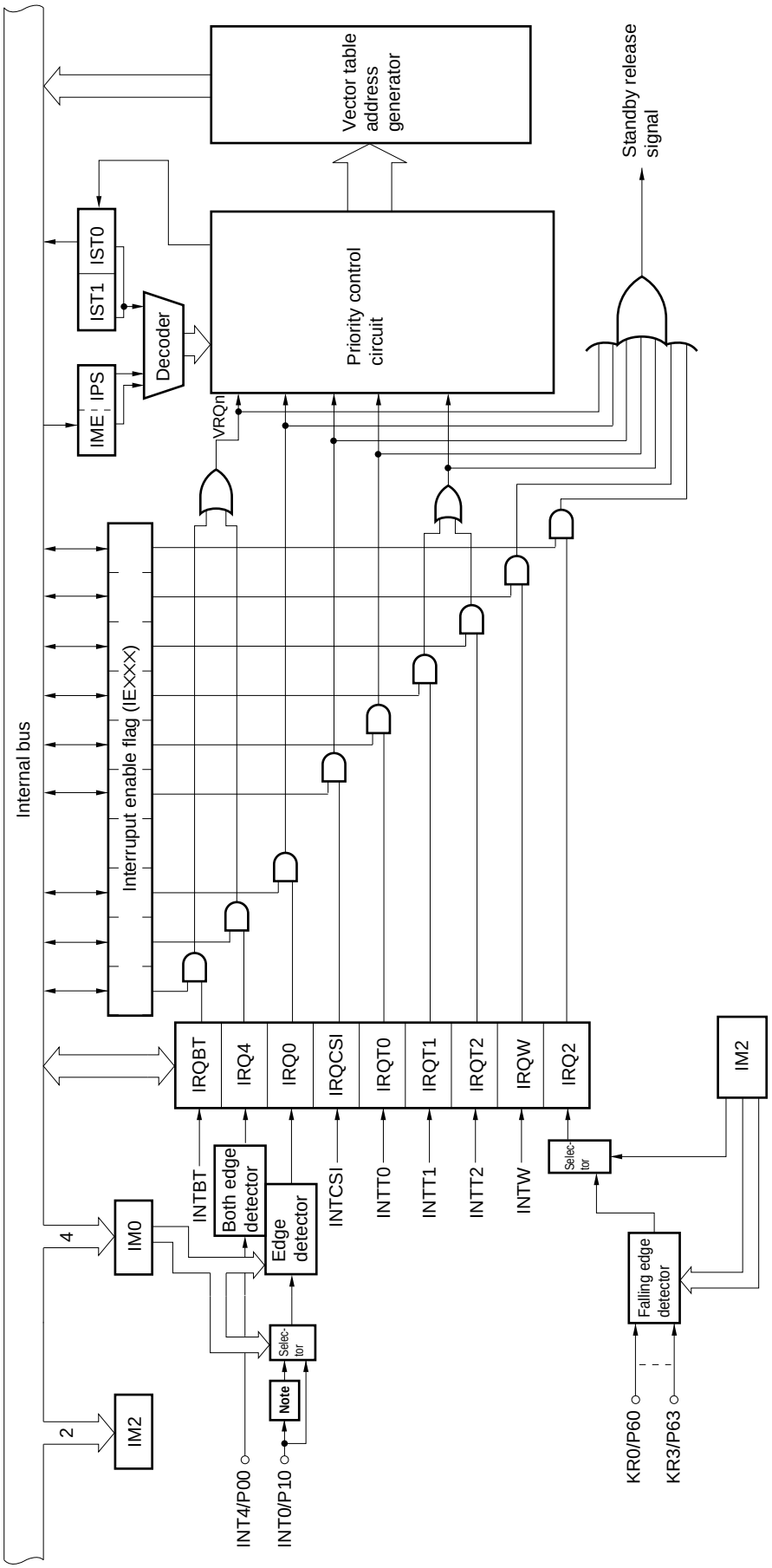



**Figure 7-1. Interrupt Control Circuit Block Diagram**

**Note** Noise eliminator (Standby release is disabled when noise eliminator is selected.)

## 8. STANDBY FUNCTION

In order to save power dissipation while a program is in standby mode, two types of standby modes (STOP mode and HALT mode) are provided for the μPD753208.

**Table 8-1. Operation Status in Standby Mode**

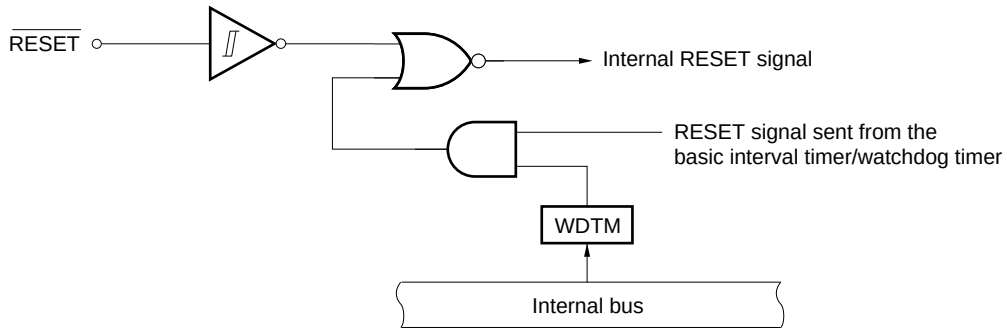
| Item \ Mode | | STOP mode | HALT mode |
|---|---|---|---|
| Set instruction | | STOP instruction | HALT instruction |
| Operation status | Clock generator | The system clock stops oscillation. | Only the CPU clock Φ halts (oscillation continues). |
| | Basic interval timer/ Watchdog timer | Operation stops. | Operable only when the system clock is oscillated. (The IRQBT is set in the reference interval). |
| | Serial interface | Operable only when an external $\overline{SCK}$ input is selected as the serial clock. | Operable |
| | Timer/event counter | Operable only when a signal input to the TI0 pin is specified as the count clock. | Operable |
| | Watch timer | Operation stops. | Operable |
| | LCD controller/driver | Operation stops. | Operable |
| | External interrupt | The INT4 is operable.<br>Only the INT0 is not operated Note. | |
| | CPU | Operation stops. | |
| Release signal | | Interrupt request signal sent from the operable hardware enabled by the interrupt enable flag or $\overline{RESET}$ signal input. | |

**Note** Can operate only when the noise eliminator is not used (IM02 = 1) by bit 2 of the edge detection mode register (IM0).

## 9. RESET FUNCTION

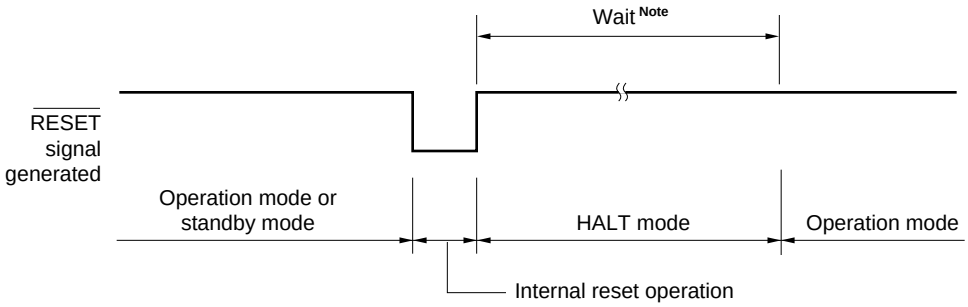
There are two reset inputs: external $\overline{\text{RESET}}$ signal and $\overline{\text{RESET}}$ signal sent from the basic interval timer/watchdog timer. When either one of the $\overline{\text{RESET}}$ signals are input, an internal $\overline{\text{RESET}}$ signal is generated. Figure 9-1 shows the circuit diagram of the above two inputs.

**Figure 9-1. Configuration of Reset Function**




Each hardware is initialized by the $\overline{\text{RESET}}$ signal generation as listed in Table 9-1. Figure 9-2 shows the timing chart of the reset operation.

**Figure 9-2. Reset Operation by $\overline{\text{RESET}}$ Signal Generation**




**Note** The following two times can be selected by the mask option.

$2^{17}/f_X$ (21.8 ms: @ 6.0-MHz operation, 31.3 ms: @ 4.19-MHz operation)

$2^{15}/f_X$ (5.46 ms: @ 6.0-MHz operation, 7.81 ms: @ 4.19-MHz operation)

**Table 9-1. Status of Each Device After Reset (1/2)**

| Hardware | | | $\overline{\text{RESET}}$ signal generation in the standby mode | $\overline{\text{RESET}}$ signal generation during operation |
|---|---|---|---|---|
| Program counter (PC) | | μPD753204 | Sets the low-order 4 bits of program memory's address 0000H to PC11 to PC8 and the contents of address 0001H to PC7 to PC0. | Sets the low-order 4 bits of program memory's address 0000H to PC11 to PC8 and the contents of address 0001H to PC7 to PC0. |
| | | μPD753206, μPD753208 | Sets the low-order 5 bits of program memory's address 0000H to PC12 to PC8 and the contents of address 0001H to PC7 to PC0. | Sets the low-order 5 bits of program memory's address 0000H to PC12 to PC8 and the contents of address 0001H to PC7 to PC0. |
| PSW | Carry flag (CY) | | Held | Undefined |
| | Skip flag (SK0-SK2) | | 0 | 0 |
| | Interrupt status flag (IST0, IST1) | | 0 | 0 |
| | Bank enable flag (MBE, RBE) | | Sets bit 6 of program memory's address 0000H to RBE and bit 7 to MBE. | Sets bit 6 of program memory's address 0000H to RBE and bit 7 to MBE. |
| Stack pointer (SP) | | | Undefined | Undefined |
| Stack bank select register (SBS) | | | 1000B | 1000B |
| ★ Data memory (RAM) | | | Held | Undefined |
| General-purpose register (X, A, H, L, D, E, B, C) | | | Held | Undefined |
| Bank select register (MBS, RBS) | | | 0, 0 | 0, 0 |
| ★ Basic interval timer/watchdog timer | Counter (BT) | | Undefined | Undefined |
| | Mode register (BTM) | | 0 | 0 |
| | Watchdog timer enable flag (WDTM) | | 0 | 0 |
| Timer/event counter (T0) | Counter (T0) | | 0 | 0 |
| | Modulo register (TMOD0) | | FFH | FFH |
| | Mode register (TM0) | | 0 | 0 |
| | TOE0, TOUT F/F | | 0, 0 | 0, 0 |
| Timer counter (T1) | Counter (T1) | | 0 | 0 |
| | Modulo register (TMOD1) | | FFH | FFH |
| | Mode register (TM1) | | 0 | 0 |
| | TOE1, TOUT F/F | | 0, 0 | 0, 0 |
| Timer counter (T2) | Counter (T2) | | 0 | 0 |
| | Modulo register (TMOD2) | | FFH | FFH |
| | High-level period setting modulo register (TMOD2H) | | FFH | FFH |
| | Mode register (TM2) | | 0 | 0 |
| | TOE2, TOUT F/F | | 0, 0 | 0, 0 |
| | REMC, NRZ, NRZB | | 0, 0, 0 | 0, 0, 0 |
| | TGCE | | 0 | 0 |
| Watch timer | Mode register (WM) | | 0 | 0 |

**Table 9-1. Status of Each Device After Reset (2/2)**

| Hardware | | $\overline{\text{RESET}}$ signal generation in the standby mode | $\overline{\text{RESET}}$ signal generation during operation |
|---|---|---|---|
| Serial interface | Shift register (SIO) | Held | Undefined |
| | Operation mode register (CSIM) | 0 | 0 |
| | SBI control register (SBIC) | 0 | 0 |
| | Slave address register (SVA) | Held | Undefined |
| Clock generator, clock output circuit | Processor clock control register (PCC) | 0 | 0 |
| | Clock output mode register (CLOM) | 0 | 0 |
| LCD controller/ driver | Display mode register (LCDM) | 0 | 0 |
| | Display control register (LCDC) | 0 | 0 |
| | LCD/port selection register (LPS) | 0 | 0 |
| Interrupt function | Interrupt request flag (IRQ×××) | Reset (0) | Reset (0) |
| | Interrupt enable flag (IE×××) | 0 | 0 |
| | Interrupt priority selection register (IPS) | 0 | 0 |
| | INT0, 2 mode registers (IM0, IM2) | 0, 0 | 0, 0 |
| Digital port | Output buffer | Off | Off |
| | Output latch | Cleared (0) | Cleared (0) |
| | I/O mode registers (PMGA, B, C) | 0 | 0 |
| | Pull-up resistor setting register (POGA, B) | 0 | 0 |
| Bit sequential buffer (BSB0 to BSB3) | | Held | Undefined |

## 10. MASK OPTION

The μPD753208 has the following mask options.

- P50 to P53 mask options
  Selects whether or not to connect an internal pull-up resistor.
  <1> Connect pull-up resistor internally bit-wise.
  <2> Do not connect pull-up resistor internally.
- $V_{LC0}$ to $V_{LC2}$ pins, BIAS pins mask option
  Selects whether or not to internally connect LCD-driving split resistors.
  <1> Do not connect split resistor internally.
  <2> Connect four 10-kΩ (typ.) split resistors simultaneously internally.
  <3> Connect four 100-kΩ (typ.) split resistors simultaneously internally.
- Standby function mask option
  Selects the wait time with the $\overline{\text{RESET}}$ signal.
  <1> $2^{17}$/fx (21.8 ms: When $f_X$ = 6.0 MHz, 31.3 ms: When $f_X$ = 4.19 MHz)
  <2> $2^{15}$/fx (5.46 ms: When $f_X$ = 6.0 MHz, 7.81 ms: When $f_X$ = 4.19 MHz)

## 11. INSTRUCTION SET

### (1) Expression formats and description methods of operands

The operand is described in the operand column of each instruction in accordance with the description method for the operand expression format of the instruction. For details, refer to **"RA75X ASSEMBLER PACKAGE USERS' MANUAL—LANGUAGE (EEU-1363)"**. If there are several elements, one of them is selected. Capital letters and the + and – symbols are key words and are described as they are.

For immediate data, appropriate numbers and labels are described.

Instead of the labels such as mem, fmem, pmem, and bit, the symbols of the registers can be described. However, there are restrictions in the labels that can be described for fmem and pmem. For details, see the user's manual.

| Representation format | Description method |
|---|---|
| reg<br>reg1 | X, A, B, C, D, E, H, L<br>X, B, C, D, E, H, L |
| rp<br>rp1<br>rp2<br>rp'<br>rp'1 | XA, BC, DE, HL<br>BC, DE, HL<br>BC, DE<br>XA, BC, DE, HL, XA', BC', DE', HL'<br>BC, DE, HL, XA', BC', DE', HL' |
| rpa<br>rpa1 | HL, HL+, HL–, DE, DL<br>DE, DL |
| n4<br>n8 | 4-bit immediate data or label<br>8-bit immediate data or label |
| mem<br>bit | 8-bit immediate data or label [Note]<br>2-bit immediate data or label |
| fmem<br>pmem | FB0H-FBFH, FF0H-FFFH immediate data or label<br>FC0H-FFFH immediate data or label |
| addr<br><br><br>addr1<br>(Only in the MKII mode)<br>caddr<br>faddr | 000H-FFFH immediate data or label (μPD753204)<br>0000H-17FFH immediate data or label (μPD753206)<br>0000H-1FFFH immediate data or label (μPD753208)<br>000H-FFFH immediate data or label (μPD753204)<br>0000H-17FFH immediate data or label (μPD753206)<br>0000H-1FFFH immediate data or label (μPD753208)<br>12-bit immediate data or label<br>11-bit immediate data or label |
| taddr | 20H-7FH immediate data (where bit 0 = 0) or label |
| PORTn<br>IE×××<br>RBn<br>MBn | PORT0-PORT3, PORT5, PORT6, PORT8, PORT9<br>IEBT, IET0-IET2, IE0, IE2, IE4, IECSI, IEW<br>RB0-RB3<br>MB0, MB1, MB15 |

**Note** mem can be only used for even address in 8-bit data processing.

**(2) Legend in explanation of operation**

| | |
|---|---|
| A | : A register, 4-bit accumulator |
| B | : B register |
| C | : C register |
| D | : D register |
| E | : E register |
| H | : H register |
| L | : L register |
| X | : X register |
| XA | : XA register pair; 8-bit accumulator |
| BC | : BC register pair |
| DE | : DE register pair |
| HL | : HL register pair |
| XA' | : XA' expanded register pair |
| BC' | : BC' expanded register pair |
| DE' | : DE' expanded register pair |
| HL' | : HL' expanded register pair |
| PC | : Program counter |
| SP | : Stack pointer |
| CY | : Carry flag, bit accumulator |
| PSW | : Program status word |
| MBE | : Memory bank enable flag |
| RBE | : Register bank enable flag |
| PORTn | : Port n (n = 0 to 3, 5, 6, 8, 9) |
| IME | : Interrupt master enable flag |
| IPS | : Interrupt priority selection register |
| IE×××| : Interrupt enable flag |
| RBS | : Register bank selection register |
| MBS | : Memory bank selection register |
| PCC | : Processor clock control register |
| . | : Separation between address and bit |
| (××) | : Contents addressed by ×× |
| ××H | : Hexadecimal data |

**(3) Explanation of symbols under addressing area column**

| | | | |
|---|---|---|---|
| *1 | MB = MBE•MBS<br>(MBS = 0, 1, 15) | | Data memory addressing |
| *2 | MB = 0 | | |
| *3 | MBE = 0 : MB = 0 (000H-07FH)<br>MB = 15 (F80H-FFFH)<br>MBE = 1 : MB = MBS (MBS = 0, 1, 15) | | |
| *4 | MB = 15, fmem = FB0H-FBFH, FF0H-FFFH | | |
| *5 | MB = 15, pmem = FC0H-FFFH | | |
| *6 | μPD753204 | addr = 000H-FFFH | Program memory addressing |
| | μPD753206 | addr = 0000H-17FFH | |
| | μPD753208 | addr = 0000H-1FFFH | |
| *7 | addr, addr1 = (Current PC) – 15 to (Current PC) – 1<br>(Current PC) + 2 to (Current PC) + 16 | | |
| *8 | μPD753204 | caddr = 000H-FFFH | |
| | μPD753206 | caddr = 0000H-0FFFH($PC_{12}$ = 0) or<br>1000H-17FFH($PC_{12}$ = 1) | |
| | μPD753208 | caddr = 0000H-0FFFH($PC_{12}$ = 0) or<br>1000H-1FFFH($PC_{12}$ = 1) | |
| *9 | faddr = 0000H-07FFH | | |
| *10 | taddr = 0020H-007FH | | |
| *11 | μPD753204 | addr1 = 000H-FFFH | |
| | μPD753206 | addr1 = 0000H-17FFH | |
| | μPD753208 | addr1 = 0000H-1FFFH | |

**Remarks 1.** MB indicates memory bank that can be accessed.

**2.** In *2, MB = 0 independently of how MBE and MBS are set.

**3.** In *4 and *5, MB = 15 independently of how MBE and MBS are set.

**4.** *6 to *11 indicate the areas that can be addressed.

**(4) Explanation of number of machine cycles column**

S denotes the number of machine cycles required by skip operation when a skip instruction is executed. The value of S varies as follows.

- When no skip is made: S = 0
- When the skipped instruction is a 1- or 2-byte instruction: S = 1
- When the skipped instruction is a 3-byte instruction [Note]: S = 2

**Note** 3-byte instruction: BR !addr, BRA !addr1, CALL !addr or CALLA !addr1 instruction

**Caution The GETI instruction is skipped in one machine cycle.**

One machine cycle is equal to one cycle of CPU clock (= $t_{CY}$); time can be selected from among four types by setting PCC.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Transfer instruction | MOV | A, #n4 | 1 | 1 | A ← n4 | | String effect A |
| | | reg1, #n4 | 2 | 2 | reg1 ← n4 | | |
| | | XA, #n8 | 2 | 2 | XA ← n8 | | String effect A |
| | | HL, #n8 | 2 | 2 | HL ← n8 | | String effect B |
| | | rp2, #n8 | 2 | 2 | rp2 ← n8 | | |
| | | A, @HL | 1 | 1 | A ← (HL) | *1 | |
| | | A, @HL+ | 1 | 2+S | A ← (HL), then L ← L+1 | *1 | L = 0 |
| | | A, @HL– | 1 | 2+S | A ← (HL), then L ← L–1 | *1 | L = FH |
| | | A, @rpa1 | 1 | 1 | A ← (rpa1) | *2 | |
| | | XA, @HL | 2 | 2 | XA ← (HL) | *1 | |
| | | @HL, A | 1 | 1 | (HL) ← A | *1 | |
| | | @HL, XA | 2 | 2 | (HL) ← XA | *1 | |
| | | A, mem | 2 | 2 | A ← (mem) | *3 | |
| | | XA, mem | 2 | 2 | XA ← (mem) | *3 | |
| | | mem, A | 2 | 2 | (mem) ← A | *3 | |
| | | mem, XA | 2 | 2 | (mem) ← XA | *3 | |
| | | A, reg | 2 | 2 | A ← reg | | |
| | | XA, rp' | 2 | 2 | XA ← rp' | | |
| | | reg1, A | 2 | 2 | reg1 ← A | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← XA | | |
| | XCH | A, @HL | 1 | 1 | A ↔ (HL) | *1 | |
| | | A, @HL+ | 1 | 2+S | A ↔ (HL), then L ← L+1 | *1 | L = 0 |
| | | A, @HL– | 1 | 2+S | A ↔ (HL), then L ← L–1 | *1 | L = FH |
| | | A, @rpa1 | 1 | 1 | A ↔ (rpa1) | *2 | |
| | | XA, @HL | 2 | 2 | XA ↔ (HL) | *1 | |
| | | A, mem | 2 | 2 | A ↔ (mem) | *3 | |
| | | XA, mem | 2 | 2 | XA ↔ (mem) | *3 | |
| | | A, reg1 | 1 | 1 | A ↔ reg1 | | |
| | | XA, rp' | 2 | 2 | XA ↔ rp' | | |

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Table reference | MOVT | XA, @PCDE | 1 | 3 | ● μPD753204<br>XA ← $(PC_{11-8}+DE)_{ROM}$ | | |
| | | | | | ● μPD753206, 753208<br>XA ← $(PC_{12-8}+DE)_{ROM}$ | | |
| | | XA, @PCXA | 1 | 3 | ● μPD753204<br>XA ← $(PC_{11-8}+XA)_{ROM}$ | | |
| | | | | | ● μPD753206, 753208<br>XA ← $(PC_{12-8}+XA)_{ROM}$ | | |
| | | XA, @BCDE | 1 | 3 | XA ← $(BCDE)_{ROM}$ Note | *6 | |
| | | XA, @BCXA | 1 | 3 | XA ← $(BCXA)_{ROM}$ Note | *6 | |
| Bit transfer | MOV1 | CY, fmem.bit | 2 | 2 | CY ← (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← $(pmem_{7-2}+L_{3-2}.bit(L_{1-0}))$ | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY ← $(H+mem_{3-0}.bit)$ | *1 | |
| | | fmem.bit, CY | 2 | 2 | (fmem.bit) ← CY | *4 | |
| | | pmem.@L, CY | 2 | 2 | $(pmem_{7-2}+L_{3-2}.bit(L_{1-0}))$ ← CY | *5 | |
| | | @H+mem.bit, CY | 2 | 2 | $(H+mem_{3-0}.bit)$ ← CY | *1 | |
| Operation | ADDS | A, #n4 | 1 | 1+S | A ← A+n4 | | carry |
| | | XA, #n8 | 2 | 2+S | XA ← XA+n8 | | carry |
| | | A, @HL | 1 | 1+S | A ← A+(HL) | *1 | carry |
| | | XA, rp' | 2 | 2+S | XA ← XA+rp' | | carry |
| | | rp'1, XA | 2 | 2+S | rp'1 ← rp'1+XA | | carry |
| | ADDC | A, @HL | 1 | 1 | A, CY ← A+(HL)+CY | *1 | |
| | | XA, rp' | 2 | 2 | XA, CY ← XA+rp'+CY | | |
| | | rp'1, XA | 2 | 2 | rp'1, CY ← rp'1+XA+CY | | |
| | SUBS | A, @HL | 1 | 1+S | A ← A–(HL) | *1 | borrow |
| | | XA, rp' | 2 | 2+S | XA ← XA–rp' | | borrow |
| | | rp'1, XA | 2 | 2+S | rp'1 ← rp'1–XA | | borrow |
| | SUBC | A, @HL | 1 | 1 | A, CY ← A–(HL)–CY | *1 | |
| | | XA, rp' | 2 | 2 | XA, CY ← XA–rp'–CY | | |
| | | rp'1, XA | 2 | 2 | rp'1, CY ← rp'1–XA–CY | | |

**Note** Set "0" to register B if the μPD753204 is used. Only the low-order one bit of register B will be valid if the μPD753206 or 753208 is used.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Operation | AND | A, #n4 | 2 | 2 | A ← A ∧ n4 | | |
| | | A, @HL | 1 | 1 | A ← A ∧ (HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA ← XA ∧ rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← rp'1 ∧ XA | | |
| | OR | A, #n4 | 2 | 2 | A ← A ∨ n4 | | |
| | | A, @HL | 1 | 1 | A ← A ∨ (HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA ← XA ∨ rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← rp'1 ∨ XA | | |
| | XOR | A, #n4 | 2 | 2 | A ← A ∀ n4 | | |
| | | A, @HL | 1 | 1 | A ← A ∀ (HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA ← XA ∀ rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← rp'1 ∀ XA | | |
| Accumulator manipulation instructions | RORC | A | 1 | 1 | CY ← $A_0$, $A_3$ ← CY, $A_{n-1}$ ← $A_n$ | | |
| | NOT | A | 2 | 2 | A ← $\overline{A}$ | | |
| Increment and Decrement instructions | INCS | reg | 1 | 1+S | reg ← reg+1 | | reg=0 |
| | | rp1 | 1 | 1+S | rp1 ← rp1+1 | | rp1=00H |
| | | @HL | 2 | 2+S | (HL) ← (HL)+1 | *1 | (HL)=0 |
| | | mem | 2 | 2+S | (mem) ← (mem)+1 | *3 | (mem)=0 |
| | DECS | reg | 1 | 1+S | reg ← reg–1 | | reg=FH |
| | | rp' | 2 | 2+S | rp' ← rp'–1 | | rp'=FFH |
| Comparison instruction | SKE | reg, #n4 | 2 | 2+S | Skip if reg = n4 | | reg=n4 |
| | | @HL, #n4 | 2 | 2+S | Skip if (HL) = n4 | *1 | (HL) = n4 |
| | | A, @HL | 1 | 1+S | Skip if A = (HL) | *1 | A = (HL) |
| | | XA, @HL | 2 | 2+S | Skip if XA = (HL) | *1 | XA = (HL) |
| | | A, reg | 2 | 2+S | Skip if A = reg | | A=reg |
| | | XA, rp' | 2 | 2+S | Skip if XA = rp' | | XA=rp' |
| Carry flag manipulation instruction | SET1 | CY | 1 | 1 | CY ← 1 | | |
| | CLR1 | CY | 1 | 1 | CY ← 0 | | |
| | SKT | CY | 1 | 1+S | Skip if CY = 1 | | CY=1 |
| | NOT1 | CY | 1 | 1 | CY ← $\overline{CY}$ | | |

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Memory bit manipulation instructions | SET1 | mem.bit | 2 | 2 | (mem.bit) ← 1 | *3 | |
| | | fmem.bit | 2 | 2 | (fmem.bit) ← 1 | *4 | |
| | | pmem.@L | 2 | 2 | (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← 1 | *5 | |
| | | @H+mem.bit | 2 | 2 | (H+mem$_{3-0}$.bit) ← 1 | *1 | |
| | CLR1 | mem.bit | 2 | 2 | (mem.bit) ← 0 | *3 | |
| | | fmem.bit | 2 | 2 | (fmem.bit) ← 0 | *4 | |
| | | pmem.@L | 2 | 2 | (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← 0 | *5 | |
| | | @H+mem.bit | 2 | 2 | (H+mem$_{3-0}$.bit) ← 0 | *1 | |
| | SKT | mem.bit | 2 | 2+S | Skip if (mem.bit)=1 | *3 | (mem.bit)=1 |
| | | fmem.bit | 2 | 2+S | Skip if (fmem.bit)=1 | *4 | (fmem.bit)=1 |
| | | pmem.@L | 2 | 2+S | Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=1 | *5 | (pmem.@L)=1 |
| | | @H+mem.bit | 2 | 2+S | Skip if (H+mem$_{3-0}$.bit)=1 | *1 | (@H+mem.bit)=1 |
| | SKF | mem.bit | 2 | 2+S | Skip if (mem.bit)=0 | *3 | (mem.bit)=0 |
| | | fmem.bit | 2 | 2+S | Skip if (fmem.bit)=0 | *4 | (fmem.bit)=0 |
| | | pmem.@L | 2 | 2+S | Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=0 | *5 | (pmem.@L)=0 |
| | | @H+mem.bit | 2 | 2+S | Skip if (H+mem$_{3-0}$.bit)=0 | *1 | (@H+mem.bit)=0 |
| | SKTCLR | fmem.bit | 2 | 2+S | Skip if (fmem.bit)=1 and clear | *4 | (fmem.bit)=1 |
| | | pmem.@L | 2 | 2+S | Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=1 and clear | *5 | (pmem.@L)=1 |
| | | @H+mem.bit | 2 | 2+S | Skip if (H+mem$_{3-0}$.bit)=1 and clear | *1 | (@H+mem.bit)=1 |
| | AND1 | CY, fmem.bit | 2 | 2 | CY ← CY ∧ (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← CY ∧ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY ← CY ∧ (H+mem$_{3-0}$.bit) | *1 | |
| | OR1 | CY, fmem.bit | 2 | 2 | CY ← CY ∨ (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← CY ∨ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY ← CY ∨ (H+mem$_{3-0}$.bit) | *1 | |
| | XOR1 | CY, fmem.bit | 2 | 2 | CY ← CY ∀ (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← CY ∀ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY ← CY ∀ (H+mem$_{3-0}$.bit) | *1 | |

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Branch instructions | BR Note | addr | – | – | • μPD753204<br>$PC_{11-0} \leftarrow$ addr<br>(Select the most appropriate instruction from among BR !addr, BRCB !caddr and BR $addr according to the assembler being used.) | *6 | |
| | | | | | • μPD753206, 753208<br>$PC_{12-0} \leftarrow$ addr<br>(Select the most appropriate instruction from among BR !addr, BRCB !caddr and BR $addr according to the assembler being used.) | | |
| | | addr1 | – | – | • μPD753204<br>$PC_{11-0} \leftarrow$ addr1<br>(Select the most appropriate instruction from among BR !addr, BRA !addr1, BRCB !caddr and BR $addr1 according to the assembler being used.) | *11 | |
| | | | | | • μPD753206, 753208<br>$PC_{12-0} \leftarrow$ addr1<br>(Select the most appropriate instruction from among BR !addr, BRA !addr1, BRCB !caddr and BR $addr1 according to the assembler being used.) | | |
| | | ! addr | 3 | 3 | • μPD753204<br>$PC_{11-0} \leftarrow$ addr | *6 | |
| | | | | | • μPD753206, 753208<br>$PC_{12-0} \leftarrow$ addr | | |
| | | $addr | 1 | 2 | • μPD753204<br>$PC_{11-0} \leftarrow$ addr | *7 | |
| | | | | | • μPD753206, 753208<br>$PC_{12-0} \leftarrow$ addr | | |
| | | $addr1 | 1 | 2 | • μPD753204<br>$PC_{11-0} \leftarrow$ addr1 | | |
| | | | | | • μPD753206, 753208<br>$PC_{12-0} \leftarrow$ addr1 | | |

**Note** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Branch instruction | BR | PCDE | 2 | 3 | • μPD753204<br>$PC_{11-0} \leftarrow PC_{11-8}$+DE | | |
| | | | | | • μPD753206, 753208<br>$PC_{12-0} \leftarrow PC_{12-8}$+DE | | |
| | | PCXA | 2 | 3 | • μPD753204<br>$PC_{11-0} \leftarrow PC_{11-8}$+XA | | |
| | | | | | • μPD753206, 753208<br>$PC_{12-0} \leftarrow PC_{12-8}$+XA | | |
| | | BCDE | 2 | 3 | • μPD753204<br>$PC_{11-0} \leftarrow$ BCDE Note 1 | *6 | |
| | | | | | • μPD753206, 753208<br>$PC_{12-0} \leftarrow$ BCDE Note 2 | | |
| | | BCXA | 2 | 3 | • μPD753204<br>$PC_{11-0} \leftarrow$ BCXA Note 1 | *6 | |
| | | | | | • μPD753206, 753208<br>$PC_{12-0} \leftarrow$ BCXA Note 2 | | |
| | BRA Note 3 | !addr1 | 3 | 3 | • μPD753204<br>$PC_{11-0} \leftarrow$ addr1 | *6 | |
| | | | | | • μPD753206, 753208<br>$PC_{12-0} \leftarrow$ addr1 | | |
| | BRCB | !caddr | 2 | 2 | • μPD753204<br>$PC_{11-0} \leftarrow caddr_{11-0}$ | *8 | |
| | | | | | • μPD753206, 753208<br>$PC_{12-0} \leftarrow PC_{12}+caddr_{11-0}$ | | |
| Subroutine stack control instructions | CALLA Note 3 | !addr1 | 3 | 3 | • μPD753204<br>(SP–2) ← ×, ×, MBE, RBE<br>(SP–6) (SP–3) (SP–4) ← $PC_{11-0}$<br>(SP–5) ← 0, 0, 0, 0<br>$PC_{11-0}$ ← addr1, SP ← SP–6 | *11 | |
| | | | | | • μPD753206, 753208<br>(SP–2) ← ×, ×, MBE, RBE<br>(SP–6) (SP–3) (SP–4) ← $PC_{11-0}$<br>(SP–5) ← 0, 0, 0, $PC_{12}$<br>$PC_{12-0}$ ← addr1, SP ← SP–6 | | |

**Notes 1.** "0" must be set to the B register.

**2.** Only the low-order one bit is valid in the B register.

**3.** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Subroutine stack control instructions | CALL Note | !addr | 3 | 3 | • μPD753204<br>(SP–3) ← MBE, RBE, 0, 0<br>(SP–4) (SP–1) (SP–2) ← $PC_{11-0}$<br>$PC_{11-0}$ ← addr, SP ← SP–4 | *6 | |
| | | | | | • μPD753206, 753208<br>(SP–3) ← MBE, RBE, 0, $PC_{12}$<br>(SP–4) (SP–1) (SP–2) ← $PC_{11-0}$<br>$PC_{12-0}$ ← addr, SP ← SP–4 | | |
| | | | | 4 | • μPD753204<br>(SP–2) ← ×, ×, MBE, RBE<br>(SP–6) (SP–3) (SP–4) ← $PC_{11-0}$<br>(SP–5) ← 0, 0, 0, 0<br>$PC_{11-0}$ ← addr, SP ← SP–6 | | |
| | | | | | • μPD753206, 753208<br>(SP–2) ← ×, ×, MBE, RBE<br>(SP–6) (SP–3) (SP–4) ← $PC_{11-0}$<br>(SP–5) ← 0, 0, 0, $PC_{12}$<br>$PC_{12-0}$ ← addr, SP ← SP–6 | | |
| | CALLF Note | !faddr | 2 | 2 | • μPD753204<br>(SP–3) ← MBE, RBE, 0, 0<br>(SP–4) (SP–1) (SP–2) ← $PC_{11-0}$<br>$PC_{11-0}$ ← 0+faddr, SP ← SP–4 | *9 | |
| | | | | | • μPD753206, 753208<br>(SP–3) ← MBE, RBE, 0, $PC_{12}$<br>(SP–4) (SP–1) (SP–2) ← $PC_{11-0}$<br>$PC_{12-0}$ ← 00+faddr, SP ← SP–4 | | |
| | | | | 3 | • μPD753204<br>(SP–2) → ×, ×, MBE, RBE<br>(SP–6) (SP–3) (SP–4) ← $PC_{11-0}$<br>(SP–5) ← 0, 0, 0, 0<br>$PC_{11-0}$ ← 0+faddr, SP ← SP–6 | | |
| | | | | | • μPD753206, 753208<br>(SP–2) → ×, ×, MBE, RBE<br>(SP–6) (SP–3) (SP–4) ← $PC_{11-0}$<br>(SP–5) ← 0, 0, 0, $PC_{12}$<br>$PC_{12-0}$ ← 00+faddr, SP ← SP–6 | | |

**Note** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Subroutine stack control instructions | RET Note | | 1 | 3 | • μPD753204<br>$PC_{11-0}$ ← (SP) (SP+3) (SP+2)<br>MBE, RBE, 0, 0 ← (SP+1), SP ← SP+4 | | |
| | | | | | • μPD753206, 753208<br>$PC_{11-0}$ ← (SP) (SP+3) (SP+2)<br>MBE, RBE, 0, $PC_{12}$ ← (SP+1), SP ← SP+4 | | |
| | | | | | • μPD753204<br>×, ×, MBE, RBE ← (SP+4)<br>0, 0, 0, 0, ← (SP+1)<br>$PC_{11-0}$ ← (SP) (SP+3) (SP+2), SP ← SP+6 | | |
| | | | | | • μPD753206, 753208<br>×, ×, MBE, RBE ← (SP+4)<br>MBE, 0, 0, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP) (SP+3) (SP+2), SP ← SP+6 | | |
| | RETS Note | | 1 | 3+S | • μPD753204<br>MBE, RBE, 0, 0 ← (SP+1)<br>$PC_{11-0}$ ← (SP) (SP+3) (SP+2)<br>SP ← SP+4<br>then skip unconditionally | | Unconditional |
| | | | | | • μPD753206, 753208<br>MBE, RBE, 0, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP) (SP+3) (SP+2)<br>SP ← SP+4<br>then skip unconditionally | | |
| | | | | | • μPD753204<br>0, 0, 0, 0 ← (SP+1)<br>$PC_{11-0}$ ← (SP) (SP+3) (SP+2)<br>×, ×, MBE, RBE ← (SP+4)<br>SP ← SP+6<br>then skip unconditionally | | |
| | | | | | • μPD753206, 753208<br>0, 0, 0, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP) (SP+3) (SP+2)<br>×, ×, MBE, RBE ← (SP+4)<br>SP ← SP+4<br>then skip unconditionally | | |

**Note** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Subroutine stack control instructions | RETI Note 1 | | 1 | 3 | • μPD753204<br>MBE, RBE, 0, 0 ← (SP+1)<br>$PC_{11-0}$ ← (SP) (SP+3) (SP+2)<br>PSW ← (SP+4) (SP+5), SP ← SP+6 | | |
| | | | | | • μPD753206, 753208<br>MBE, RBE, 0, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP) (SP+3) (SP+2)<br>PSW ← (SP+4) (SP+5), SP ← SP+6 | | |
| | | | | | • μPD753204<br>0, 0, 0, 0 ← (SP+1)<br>$PC_{11-0}$ ← (SP) (SP+3) (SP+2)<br>PSW ← (SP+4) (SP+5), SP ← SP+6 | | |
| | | | | | • μPD753206, 753208<br>0, 0, 0, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP) (SP+3) (SP+2)<br>PSW ← (SP+4) (SP+5), SP ← SP+6 | | |
| | PUSH | rp | 1 | 1 | (SP–1)(SP–2) ← rp, SP ← SP–2 | | |
| | | BS | 2 | 2 | (SP–1) ← MBS, (SP–2) ← RBS, SP ← SP–2 | | |
| | POP | rp | 1 | 1 | rp ← (SP+1) (SP), SP ← SP+2 | | |
| | | BS | 2 | 2 | MBS ← (SP+1), RBS ← (SP), SP ← SP+2 | | |
| Interrupt control instructions | EI | | 2 | 2 | IME (IPS.3) ← 1 | | |
| | | IE×××| 2 | 2 | IE××× ← 1 | | |
| | DI | | 2 | 2 | IME (IPS.3) ← 0 | | |
| | | IE××× | 2 | 2 | IE××× ← 0 | | |
| Input/output instructions | IN Note 2 | A, PORTn | 2 | 2 | A ← PORTn (n = 0-3, 5, 6, 8, 9) | | |
| | | XA, PORTn | 2 | 2 | XA ← PORTn+1, PORTn (n = 8) | | |
| | OUT Note 2 | PORTn, A | 2 | 2 | PORTn ← A (n = 3, 5, 6, 8, 9) | | |
| | | PORTn, XA | 2 | 2 | PORTn+1, PORTn ← XA (n = 8) | | |
| CPU control instructions | HALT | | 2 | 2 | Set HALT Mode (PCC.2 ← 1) | | |
| | STOP | | 2 | 2 | Set STOP Mode (PCC.3 ← 1) | | |
| | NOP | | 1 | 1 | No Operation | | |
| Special instructions | SEL | RBn | 2 | 2 | RBS ← n (n = 0-3) | | |
| | | MBn | 2 | 2 | MBS ← n (n = 0, 1, 15) | | |

**Notes 1.** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

**2.** While the IN instruction and OUT instruction are being executed, the MBE must be set to 0 or 1 and MBS must be set to 15.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Special instructions | GET Notes 1, 2 | taddr | 1 | 3 | • μPD753204<br>• When TBR instruction<br>$PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$ | *10 | |
| | | | | | • When TCALL instruction<br>$(SP-4)\ (SP-1)\ (SP-2) \leftarrow PC_{11-0}$<br>$(SP-3) \leftarrow MBE, RBE, 0, 0$<br>$PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$<br>$SP \leftarrow SP-4$ | | |
| | | | | | • When instruction other than TBR and TCALL instructions<br>(taddr) (taddr+1) instruction is executed. | | Depending on the reference instruction |
| | | | | | • μPD753206, 753208<br>• When TBR instruction<br>$PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr+1)$ | | |
| | | | | | • When TCALL instruction<br>$(SP-4)\ (SP-1)\ (SP-2) \leftarrow PC_{11-0}$<br>$(SP-3) \leftarrow MBE, RBE, 0, PC_{12}$<br>$PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr+1)$<br>$SP \leftarrow SP-4$ | | |
| | | | | | • When instruction other than TBR and TCALL instructions<br>(taddr) (taddr+1) instruction is executed. | | Depending on the reference instruction |
| | | | | 3 | • μPD753204<br>• When TBR instruction<br>$PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$ | *10 | |
| | | | | 4 | • When TCALL instruction<br>$(SP-6)\ (SP-3)\ (SP-4) \leftarrow PC_{11-0}$<br>$(SP-5) \leftarrow 0, 0, 0, 0$<br>$(SP-2) \leftarrow \times, \times, MBE, RBE$<br>$PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$<br>$SP \leftarrow SP-6$ | | |
| | | | | 3 | • When instruction other than TBR and TCALL instructions<br>(taddr) (taddr+1) instruction is executed. | | Depending on the reference instruction |

**Notes 1.** The TBR and TCALL instructions are the table definition assembler pseudo instructions of the GETI instruction.

**2.** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Special instructions | GETI Notes 1, 2 | taddr | 1 | 3 | • μPD753206, 753208<br>• When TBR instruction<br>$PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr+1)$ | *10 | |
| | | | | 4 | • When TCALL instruction<br>(SP–6) (SP–3) (SP–4) ← $PC_{11-0}$<br>(SP–5) ← 0, 0, 0, $PC_{12}$<br>(SP–2) ← ×, ×, MBE, RBE<br>$PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr+1)$<br>SP ← SP–6 | | |
| | | | | 3 | • When instruction other than TBR and TCALL instructions<br>(taddr) (taddr+1) instruction is executed. | | Depending on the reference instruction |

**Notes 1.** The TBR and TCALL instructions are the table definition assembler pseudo instructions of the GETI instruction.

**2.** The above operations in the double boxes can be performed only in the Mk II mode.

## 12. ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C)

| Parameter | Symbol | Test Conditions | | Rating | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | | –0.3 to +7.0 | V |
| Input voltage | $V_{I1}$ | Except port 5 | | –0.3 to $V_{DD}$ + 0.3 | V |
| | $V_{I2}$ | Port 5 | On-chip pull-up resistor | –0.3 to $V_{DD}$ + 0.3 | V |
| | | | When N-ch open-drain | –0.3 to +14 | V |
| Output voltage | $V_O$ | | | –0.3 to $V_{DD}$ + 0.3 | V |
| Output current high | $I_{OH}$ | Per pin | | –10 | mA |
| | | Total for all pins | | –30 | mA |
| Output current low | $I_{OL}$ | Per pin | | 30 | mA |
| | | Total for all pins | | 220 | mA |
| Operating ambient temperature | $T_A$ | | | –40 to +85 Note | °C |
| Storage temperature | $T_{stg}$ | | | –65 to +150 | °C |

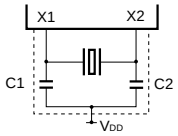
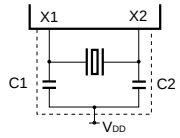
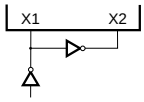
**Note** When LCD is driven in normal mode: $T_A$ = –10 to +85°C

**Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.**

### CAPACITANCE ($T_A$ = 25°C, $V_{DD}$ = 0 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | f = 1 MHz | | | 15 | pF |
| Output capacitance | $C_{OUT}$ | Unmeasured pins returned to 0 V. | | | 15 | pF |
| I/O capacitance | $C_{IO}$ | | | | 15 | pF |

**SYSTEM CLOCK OSCILLATOR CHARACTERISTICS ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Resonator | Recommended constant | Parameter | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Ceramic resonator |  | Oscillator frequency ($f_X$) Note 1 | | 1.0 | | 6.0 Note 2 | MHz |
| | | Oscillation stabilization time Note 3 | After $V_{DD}$ reaches oscillation voltage range MIN. | | | 4 | ms |
| Crystal resonator |  | Oscillator frequency ($f_X$) Note 1 | | 1.0 | | 6.0 Note 2 | MHz |
| | | Oscillation stabilization time Note 3 | $V_{DD}$ = 4.5 to 5.5 V | | | 10 | ms |
| | | | | | | 30 | |
| External clock |  | X1 input frequency ($f_X$) Note 1 | | 1.0 | | 6.0 Note 2 | MHz |
| ★ | | X1 input high/low level width ($t_{XH}$, $t_{XL}$) | | 83.3 | | 500 | ns |

**Notes 1.** The oscillator frequency and X1 input frequency indicate characteristics of the oscillator only. For the instruction execution time, refer to the AC characteristics.

**2.** When the oscillator frequency is 4.19 MHz < fx ≤ 6.0 MHz, setting the processor clock control register (PCC) to 0011 results in 1 machine cycle being less than the required 0.95 μs. Therefore, set PCC to a value other than 0011.

**3.** The oscillation stabilization time is necessary for oscillation to stabilize after applying $V_{DD}$ or releasing the STOP mode.

**Caution When using the system clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.**

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as $V_{DD}$.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

★ **RECOMMENDED OSCILLATOR CONSTANTS**

**Ceramic resonator (TA = –40 to 85°C)**

| Manufacturer | Part number | Frequency (MHz) | Oscillator constant (pF) | | Oscillation voltage range ($V_{DD}$) | | Remark |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2 | MIN. (V) | MAX. (V) | |
| TDK | CCR1000K2 | 1.0 | 100 | 100 | 1.8 | 5.5 | — |
| | CCR2.0MC33 | 2.0 | — | — | 2.0 | | On-chip capacitor |
| | CCR3.58MC3 | 3.58 | | | | | |
| | CCR4.19MC3 | 4.19 | | | | | |
| | FCR4.19MC5 | | | | 2.2 | | |
| | CCR6.0MC3 | 6.0 | | | | | |
| | FCR6.0MC5 | | | | 2.5 | | |

**Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillaiton frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.**

**DC CHARACTERISTICS ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| | Parameter | Symbol | Test conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| ★ | Output voltage low | $I_{OL}$ | Per pin | | | | | 15 | mA |
| | | | Sum of the all pins | | | | | 150 | mA |
| | Input voltage high | $V_{IH1}$ | Ports 2, 3, 8, and 9 | | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | | | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0.9$V_{DD}$ | | $V_{DD}$ | V |
| | | $V_{IH2}$ | Ports 0, 1, 6, $\overline{\text{RESET}}$ | | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | | | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0.9$V_{DD}$ | | $V_{DD}$ | V |
| | | $V_{IH3}$ | Port 5 | When a pull-up register is incorporated | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | | | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0.9$V_{DD}$ | | $V_{DD}$ | V |
| | | | | When N-ch open-drain | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0.7$V_{DD}$ | | 13 | V |
| | | | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0.9$V_{DD}$ | | 13 | V |
| | | $V_{IH4}$ | X1 | | | $V_{DD}$ – 0.1 | | $V_{DD}$ | V |
| | Input voltage low | $V_{IL1}$ | Ports 2, 3, 5, 8, and 9 | | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0 | | 0.3$V_{DD}$ | V |
| | | | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0 | | 0.1$V_{DD}$ | V |
| | | $V_{IL2}$ | Ports 0, 1, 6, $\overline{\text{RESET}}$ | | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0 | | 0.2$V_{DD}$ | V |
| | | | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0 | | 0.1$V_{DD}$ | V |
| | | $V_{IL3}$ | X1 | | | 0 | | 0.1 | V |
| | Output voltage high | $V_{OH}$ | $\overline{\text{SCK}}$, SO, ports 2, 3, 6, 8, and 9 | | $I_{OH}$ = –1.0 mA | $V_{DD}$ – 0.5 | | | V |
| | Output voltage low | $V_{OL1}$ | $\overline{\text{SCK}}$, SO, ports 2, 3, 5, 6, 8, and 9 | | $I_{OL}$ = 15 mA, $V_{DD}$ = 4.5 to 5.5 V | | 0.2 | 2.0 | V |
| | | | | | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| | | $V_{OL2}$ | SB0, SB1 | N-ch open-drain pull-up resistor ≥ 1 kΩ | | | | 0.2$V_{DD}$ | V |
| | Input leakage current high | $I_{LIH1}$ | $V_{IN}$ = $V_{DD}$ | Other pins than X1 | | | | 3 | μA |
| | | $I_{LIH2}$ | | X1 | | | | 20 | μA |
| | | $I_{LIH3}$ | $V_{IN}$ = 13 V | Port 5 (When N-ch open-drain) | | | | 20 | μA |
| | Input leakage current low | $I_{LIL1}$ | $V_{IN}$ = 0 V | Other pins than port 5 and X1 | | | | –3 | μA |
| | | $I_{LIL2}$ | | X1 | | | | –20 | μA |
| ★ | | $I_{LIL3}$ | | Port 5 (When N-ch open drain) Other than when an input instruction is executed | | | | –3 | μA |
| | | | | Port 5 (When N-ch open-drain) When an input instruction is executed | | | | –30 | μA |
| | | | | | $V_{DD}$ = 5.0 V | | –10 | –27 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | –3 | –8 | μA |
| | Output leakage current high | $I_{LOH1}$ | $V_{OUT}$ = $V_{DD}$ | $\overline{\text{SCK}}$, SO/SB0, SB1, ports 2, 3, 6, 8 and 9 Port 5 (When a pull-up resistor is incorporated.) | | | | 3 | μA |
| | | $I_{LOH2}$ | $V_{OUT}$ = 13 V | Port 5 (When N-ch open-drain) | | | | 20 | μA |
| | Output leakage current low | $I_{LOL}$ | $V_{OUT}$ = 0 V | | | | | –3 | μA |
| | On-chip pull-up resistor | $R_{L1}$ | $V_{IN}$ = 0 V | Ports 0 to 3, 6, 8, and 9 (Excluding P00 pin) | | 50 | 100 | 200 | kΩ |
| | | $R_{L2}$ | | Port 5 (Mask option) | | 15 | 30 | 60 | kΩ |

**DC CHARACTERISTICS ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| | Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| ★ | LCD drive voltage | $V_{LCD}$ | VAC0 = 0 | $T_A$ = –40 to +85°C | 2.7 | | $V_{DD}$ | V |
| | | | | $T_A$ = –10 to +85°C | 2.2 | | $V_{DD}$ | V |
| | | | VAC0 = 1 | | 1.8 | | $V_{DD}$ | V |
| ★ | VAC current Note 1 | $I_{VAC}$ | VAC0 = 1, $V_{DD}$ = 2.0 V ± 10% | | | 1 | 4 | μA |
| | LCD split resistor Note 2 | $R_{LCD1}$ | | | 50 | 100 | 200 | kΩ |
| | | $R_{LCD2}$ | | | 5 | 10 | 20 | kΩ |
| | LCD output voltage deviation Note 3 (common) | $V_{ODC}$ | $I_O$ = ±1.0 μA | $V_{LCD0} = V_{LCD}$<br>$V_{LCD1} = V_{LCD} \times 2/3$<br>$V_{LCD2} = V_{LCD} \times 1/3$<br>1.8 V ≤ $V_{LCD}$ ≤ $V_{DD}$ | 0 | | ±0.2 | V |
| | LCD output voltage deviation Note 3 (segment) | $V_{ODS}$ | $I_O$ = ±0.5 μA | | 0 | | ±0.2 | V |
| | Supply current Note 4 | $I_{DD1}$ | 6.0 MHz Crystal oscillation C1 = C2 = 22 pF | $V_{DD}$ = 5.0 V ± 10% Note 5 | | 1.9 | 6.0 | mA |
| | | | | $V_{DD}$ = 3.0 V ± 10% Note 6 | | 0.4 | 1.3 | mA |
| | | $I_{DD2}$ | | HALT mode $V_{DD}$ = 5.0 V ±10% | | 0.72 | 2.1 | mA |
| | | | | HALT mode $V_{DD}$ = 3.0 V ±10% | | 0.27 | 0.8 | mA |
| | | $I_{DD1}$ | 4.19 MHz Crystal oscillation C1 = C2 = 22 pF | $V_{DD}$ = 5.0 V ± 10% Note 5 | | 1.5 | 4.0 | mA |
| | | | | $V_{DD}$ = 3.0 V ± 10% Note 6 | | 0.25 | 0.75 | mA |
| | | $I_{DD2}$ | | HALT mode $V_{DD}$ = 5.0 V ±10% | | 0.7 | 2.0 | mA |
| | | | | HALT mode $V_{DD}$ = 3.0 V ±10% | | 0.23 | 0.7 | mA |
| | | $I_{DD3}$ | STOP mode | $V_{DD}$ = 5.0 V ±10% | | 0.05 | 10 | μA |
| | | | | $V_{DD}$ = 3.0 V ±10% | | 0.02 | 5 | μA |
| | | | | $T_A$ = 25°C | | 0.02 | 3 | μA |

**Notes 1.** Set VAC0 to 0 when setting the STOP mode. If VAC0 is set to 1, the current increases by about 1 μA.

**2.** Either $R_{LCD1}$ or $R_{LCD2}$ can be selected by the mask option.

**3.** The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs ($V_{LCDn}$; n = 0, 1, 2).

**4.** Not including currents flowing in on-chip pull-up resistors or LCD split resistors.

**5.** When the processor clock control register (PCC) is set to 0011 and the device is operated in the high-speed mode.

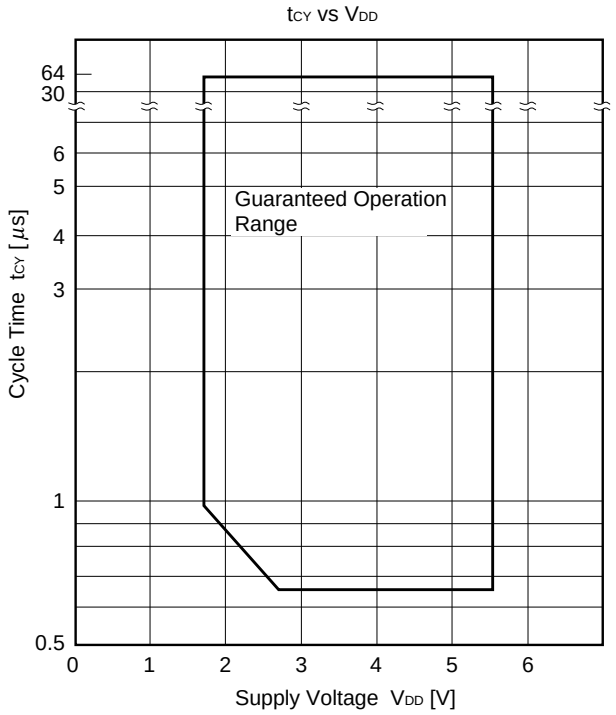
**6.** When PCC is set to 0000 and the device is operated in the low-speed mode.

**AC CHARACTERISTICS ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| CPU clock cycle time Note 1 | $t_{CY}$ | $V_{DD}$ = 2.7 to 5.5 V | | 0.67 | | 64 | μs |
| | | | | 0.95 | | 64 | μs |
| TI0 input frequency | $f_{TI}$ | $V_{DD}$ = 2.7 to 5.5 V | | 0 | | 1.0 | MHz |
| | | | | 0 | | 275 | kHz |
| TI0 input high/low-level width | $t_{TIH}$, $t_{TIL}$ | $V_{DD}$ = 2.7 to 5.5 V | | 0.48 | | | μs |
| | | | | 1.8 | | | μs |
| Interrupt input high/low-level width | $t_{INTH}$, $t_{INTL}$ | INT0 | IM02 = 0 | Note 2 | | | μs |
| | | | IM02 = 1 | 10 | | | μs |
| | | INT4 | | 10 | | | μs |
| | | KR0 to KR3 | | 10 | | | μs |
| $\overline{\text{RESET}}$ low level width | $t_{RSL}$ | | | 10 | | | μs |

**Notes 1.** The cycle time (minimum instruction execution time) of the CPU clock (Φ) is determined by the oscillation frequency of the connected resonator (and external clock) and the processor clock control register (PCC). The figure at the right indicates the cycle time $t_{CY}$ versus supply voltage $V_{DD}$ characteristic.

**2.** $2t_{CY}$ or $128/f_X$ is set by setting the interrupt mode register (IM0).



## SERIAL TRANSFER OPERATION

**2-Wire and 3-Wire Serial I/O Mode ($\overline{SCK}$...Internal clock output): ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 1300 | | | ns |
| | | | | 3800 | | | ns |
| $\overline{SCK}$ high/low-level width | $t_{KL1}$, $t_{KH1}$ | $V_{DD}$ = 2.7 to 5.5 V | | $t_{KCY1}$/2 – 50 | | | ns |
| | | | | $t_{KCY1}$/2 – 150 | | | ns |
| SI[Note 1] setup time (to $\overline{SCK}\uparrow$) | $t_{SIK1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 150 | | | ns |
| | | | | 500 | | | ns |
| SI[Note 1] hold time (from $\overline{SCK}\uparrow$) | $t_{KSI1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | | | 600 | | | ns |
| SO[Note 1] output delay time from $\overline{SCK}\downarrow$ | $t_{KSO1}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF [Note 2] | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 250 | ns |
| | | | | 0 | | 1000 | ns |

**Notes 1.** In the 2-wire serial I/O mode, read SB0 or SB1 instead.

**2.** $R_L$ and $C_L$ are the load resistance and load capacitance of the SO output lines.

**2-Wire and 3-Wire Serial I/O Mode ($\overline{SCK}$...External clock input): ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 800 | | | ns |
| | | | | 3200 | | | ns |
| $\overline{SCK}$ high/low-level width | $t_{KL2}$, $t_{KH2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | | | 1600 | | | ns |
| SI[Note 1] setup time (to $\overline{SCK}\uparrow$) | $t_{SIK2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 100 | | | ns |
| | | | | 150 | | | ns |
| SI[Note 1] hold time (from $\overline{SCK}\uparrow$) | $t_{KSI2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | | | 600 | | | ns |
| SO[Note 1] output delay time from $\overline{SCK}\downarrow$ | $t_{KSO2}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF [Note 2] | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 300 | ns |
| | | | | 0 | | 1000 | ns |

**Notes 1.** In the 2-wire serial I/O mode, read SB0 or SB1 instead.

**2.** $R_L$ and $C_L$ are the load resistance and load capacitance of the SO output lines.

**SBI Mode ($\overline{SCK}$...Internal clock output (master)): ($T_A$ = –40 to +85 °C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY3}$ | $V_{DD}$ = 2.7 to 5.5 V | | 1300 | | | ns |
| | | | | 3800 | | | ns |
| $\overline{SCK}$ high/low-level width | $t_{KL3}$, $t_{KH3}$ | $V_{DD}$ = 2.7 to 5.5 V | | $t_{KCY3}$/2 – 50 | | | ns |
| | | | | $t_{KCY3}$/2 – 150 | | | ns |
| SB0, 1 setup time (to $\overline{SCK}$↑) | $t_{SIK3}$ | $V_{DD}$ = 2.7 to 5.5 V | | 150 | | | ns |
| | | | | 500 | | | ns |
| SB0, 1 hold time (from $\overline{SCK}$↑) | $t_{KSI3}$ | $V_{DD}$ = 2.7 to 5.5 V | | $t_{KCY3}$/2 | | | ns |
| SB0, 1 output delay time from $\overline{SCK}$↓ | $t_{KSO3}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF | Note $V_{DD}$ = 2.7 to 5.5 V | 0 | | 250 | ns |
| | | | | 0 | | 1000 | ns |
| SB0, 1↓ from $\overline{SCK}$↑ | $t_{KSB}$ | | | $t_{KCY3}$ | | | ns |
| $\overline{SCK}$↓ from SB0, 1↑ | $t_{SBK}$ | | | $t_{KCY3}$ | | | ns |
| SB0, 1 low-level width | $t_{SBL}$ | | | $t_{KCY3}$ | | | ns |
| SB0, 1 high-level width | $t_{SBH}$ | | | $t_{KCY3}$ | | | ns |

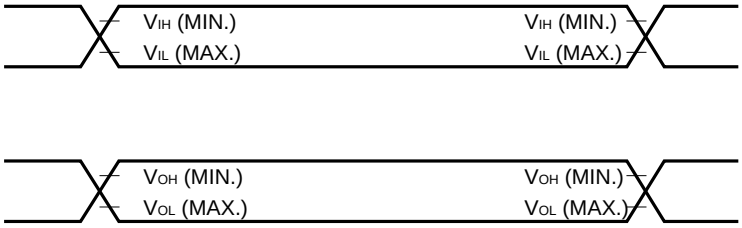
**Note** $R_L$ and $C_L$ are the load resistance and load capacitance of the SB0 and SB1 output lines.

**SBI Mode ($\overline{SCK}$...External clock input (slave)): ($T_A$ = –40 to +85 °C, $V_{DD}$ = 1.8 to 5.5 V)**

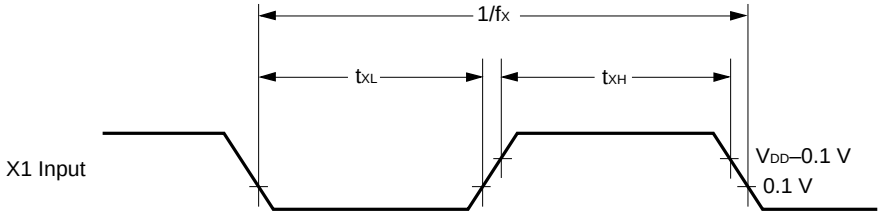
| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY4}$ | $V_{DD}$ = 2.7 to 5.5 V | | 800 | | | ns |
| | | | | 3200 | | | ns |
| $\overline{SCK}$ high/low-level width | $t_{KL4}$, $t_{KH4}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | | | 1600 | | | ns |
| SB0, 1 setup time (to $\overline{SCK}$↑) | $t_{SIK4}$ | $V_{DD}$ = 2.7 to 5.5 V | | 100 | | | ns |
| | | | | 150 | | | ns |
| SB0, 1 hold time (from $\overline{SCK}$↑) | $t_{KSI4}$ | $V_{DD}$ = 2.7 to 5.5 V | | $t_{KCY4}$/2 | | | ns |
| SB0, 1 output delay time from $\overline{SCK}$↓ | $t_{KSO4}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF | Note $V_{DD}$ = 2.7 to 5.5 V | 0 | | 300 | ns |
| | | | | 0 | | 1000 | ns |
| SB0, 1↓ from $\overline{SCK}$↑ | $t_{KSB}$ | | | $t_{KCY4}$ | | | ns |
| $\overline{SCK}$↓ from SB0, 1↑ | $t_{SBK}$ | | | $t_{KCY4}$ | | | ns |
| SB0, 1 low-level width | $t_{SBL}$ | | | $t_{KCY4}$ | | | ns |
| SB0, 1 high-level width | $t_{SBH}$ | | | $t_{KCY4}$ | | | ns |

**Note** $R_L$ and $C_L$ are the load resistance and load capacitance of the SB0 and SB1 output lines.

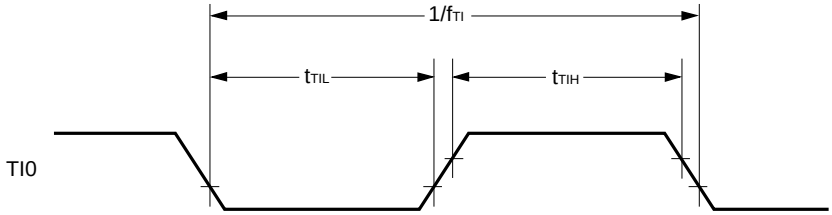
★ **AC Timing Test Point (Excluding X1 Input)**




**Clock Timing**

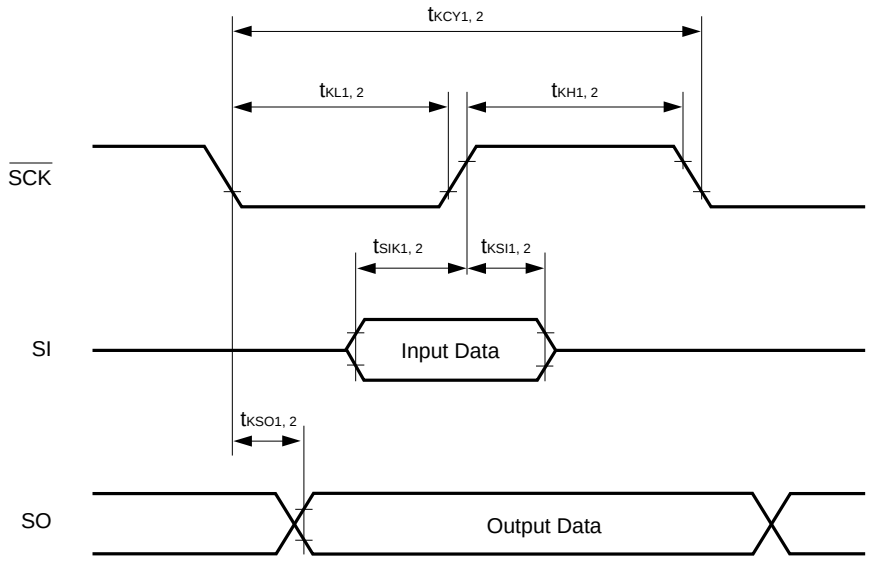



**TI0 Timing**

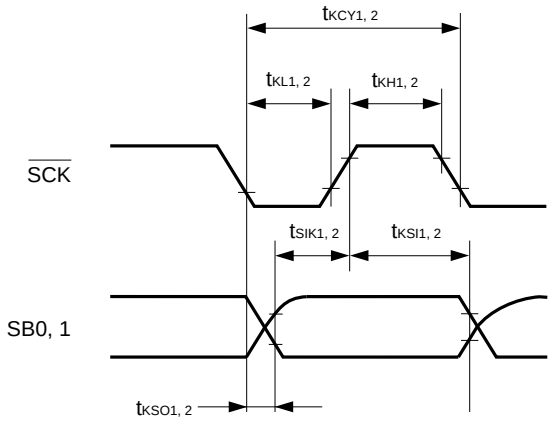


**Serial Transfer Timing**

**3-wire serial I/O mode**

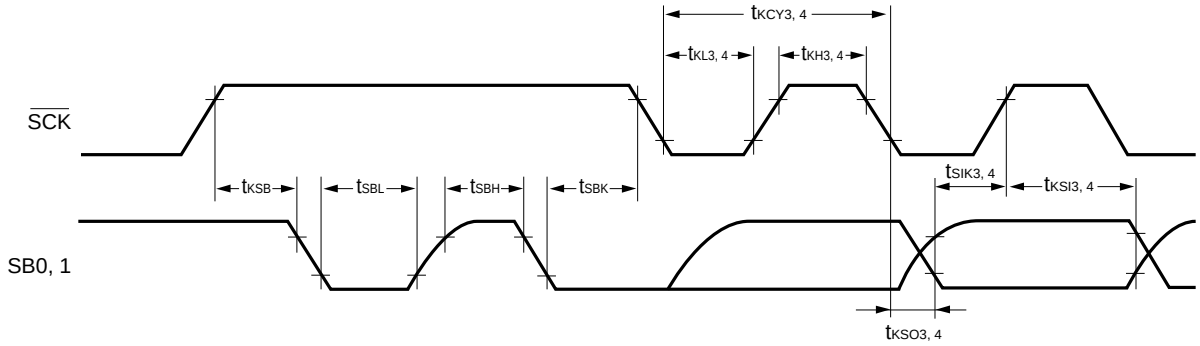



**2-wire serial I/O mode**

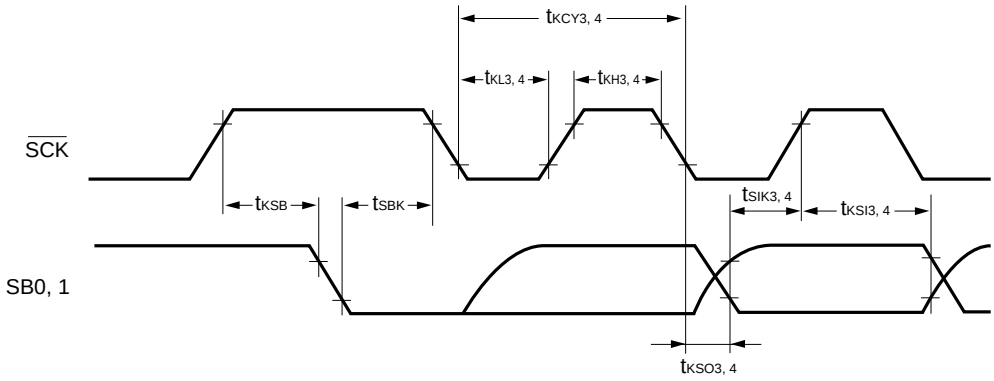


### Serial Transfer Timing

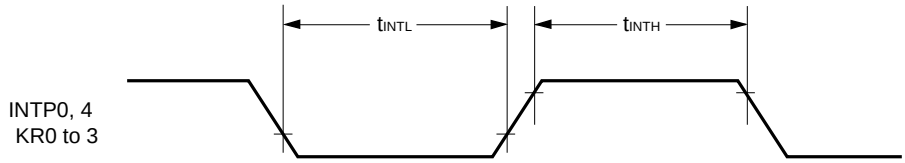
#### Bus release signal transfer



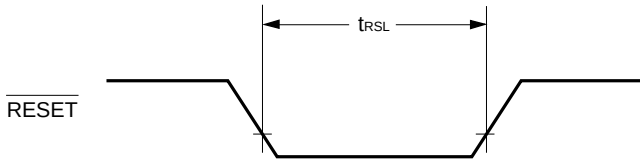

#### Command signal transfer




### Interrupt input timing




### RESET input timing



**DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS**

**($T_A$ = –40 to +85°C)**

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Release signal set time | $t_{SREL}$ | | 0 | | | μs |
| Oscillation stabilization wait time Note 1 | $t_{WAIT}$ | Release by $\overline{RESET}$ | | Note 2 | | ms |
| | | Release by interrupt | | Note 3 | | ms |

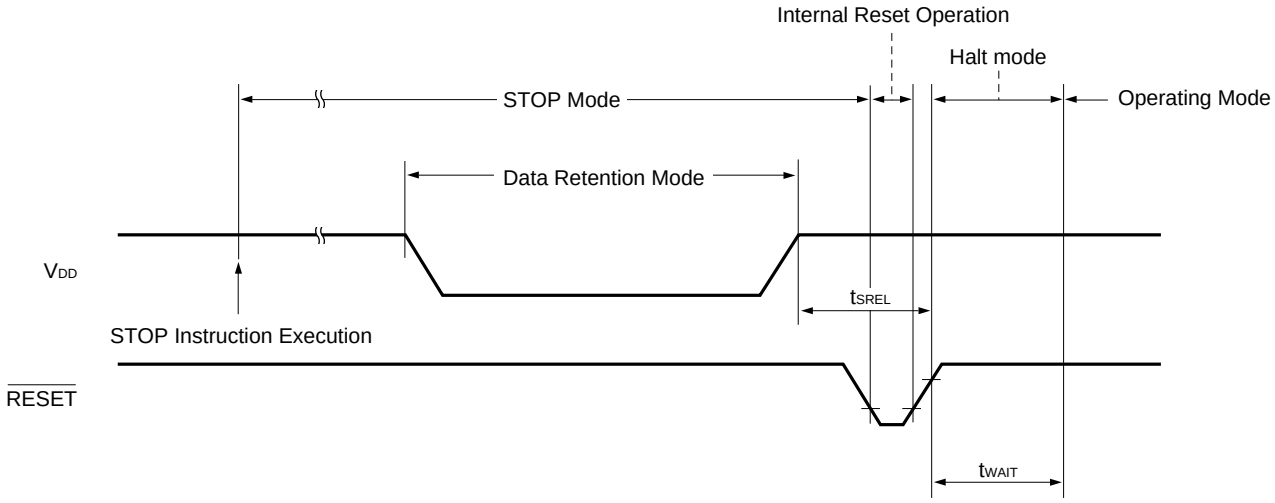
**Notes 1.** The oscillation stabillization wait time is the time during which the CPU operation is stopped to prevent unstable operation at the oscillation start.

**2.** Either $2^{17}/f_X$ or $2^{15}/f_X$ can be selected by the mask option.

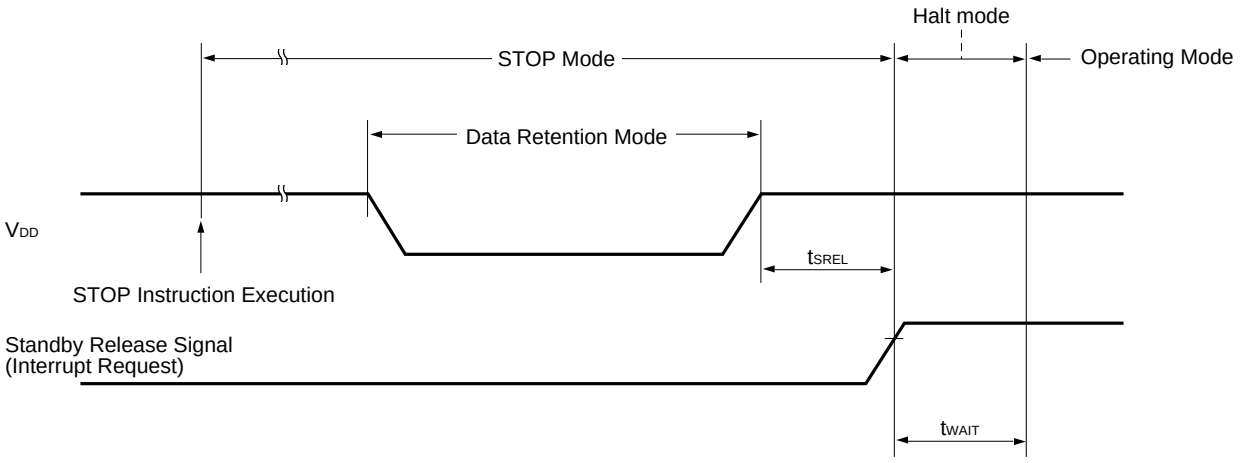
**3.** Depends on the basic interval timer mode register (BTM) settings (See the table below).

| BTM3 | BTM2 | BTM1 | BTM0 | Wait time | |
|---|---|---|---|---|---|
| | | | | When fx = 4.19-MHz operation | When fx = 6.0-MHz operation |
| — | 0 | 0 | 0 | $2^{20}/f_X$ (approx. 250 ms) | $2^{20}/f_X$ (approx. 175 ms) |
| — | 0 | 1 | 1 | $2^{17}/f_X$ (approx. 31.3 ms) | $2^{17}/f_X$ (approx. 21.8 ms) |
| — | 1 | 0 | 1 | $2^{15}/f_X$ (approx. 7.81 ms) | $2^{15}/f_X$ (approx. 5.46 ms) |
| — | 1 | 1 | 1 | $2^{13}/f_X$ (approx. 1.95 ms) | $2^{13}/f_X$ (approx. 1.37 ms) |

**Data Retention Timing (STOP Mode Release by $\overline{RESET}$)**

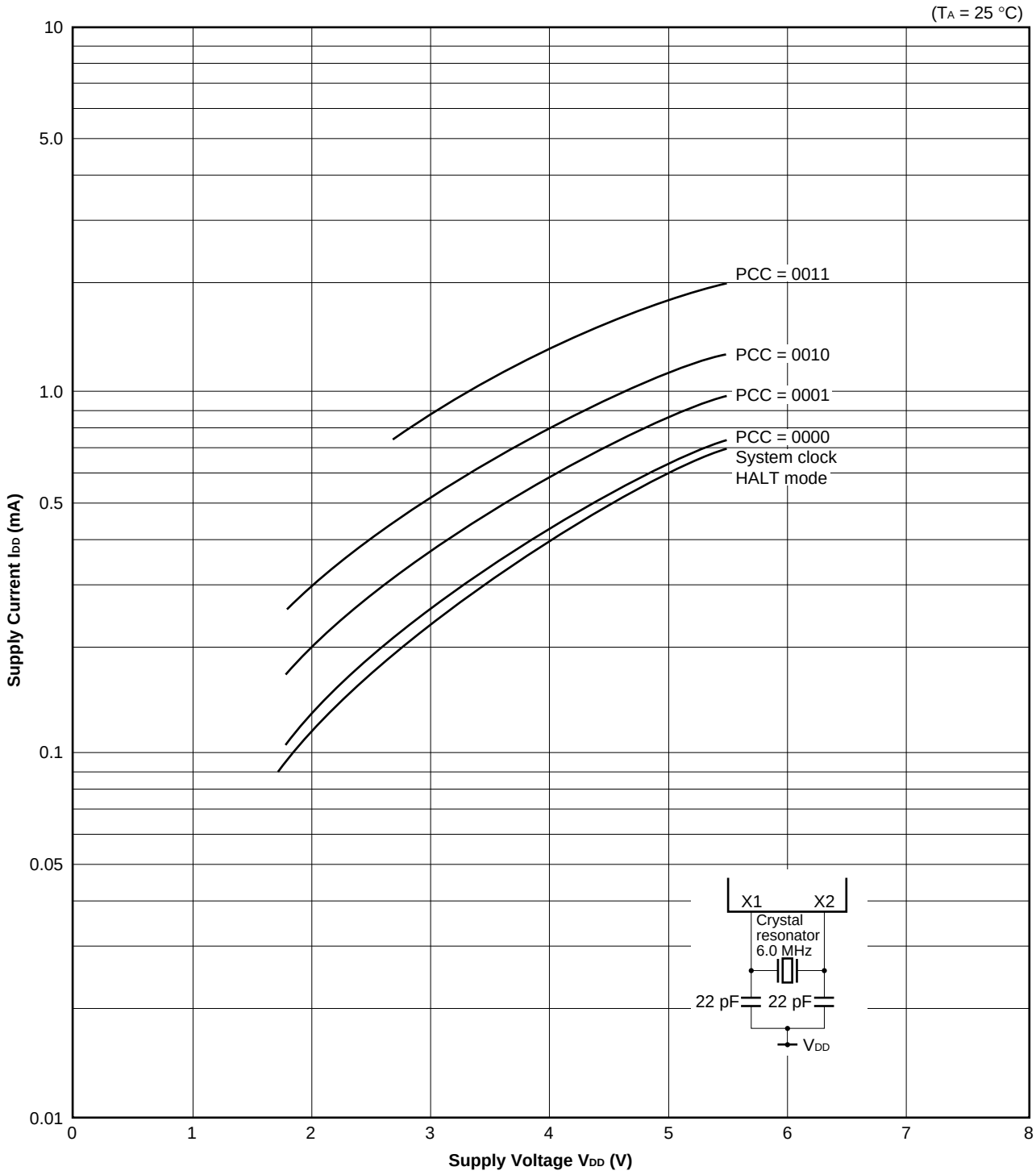



**Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)**

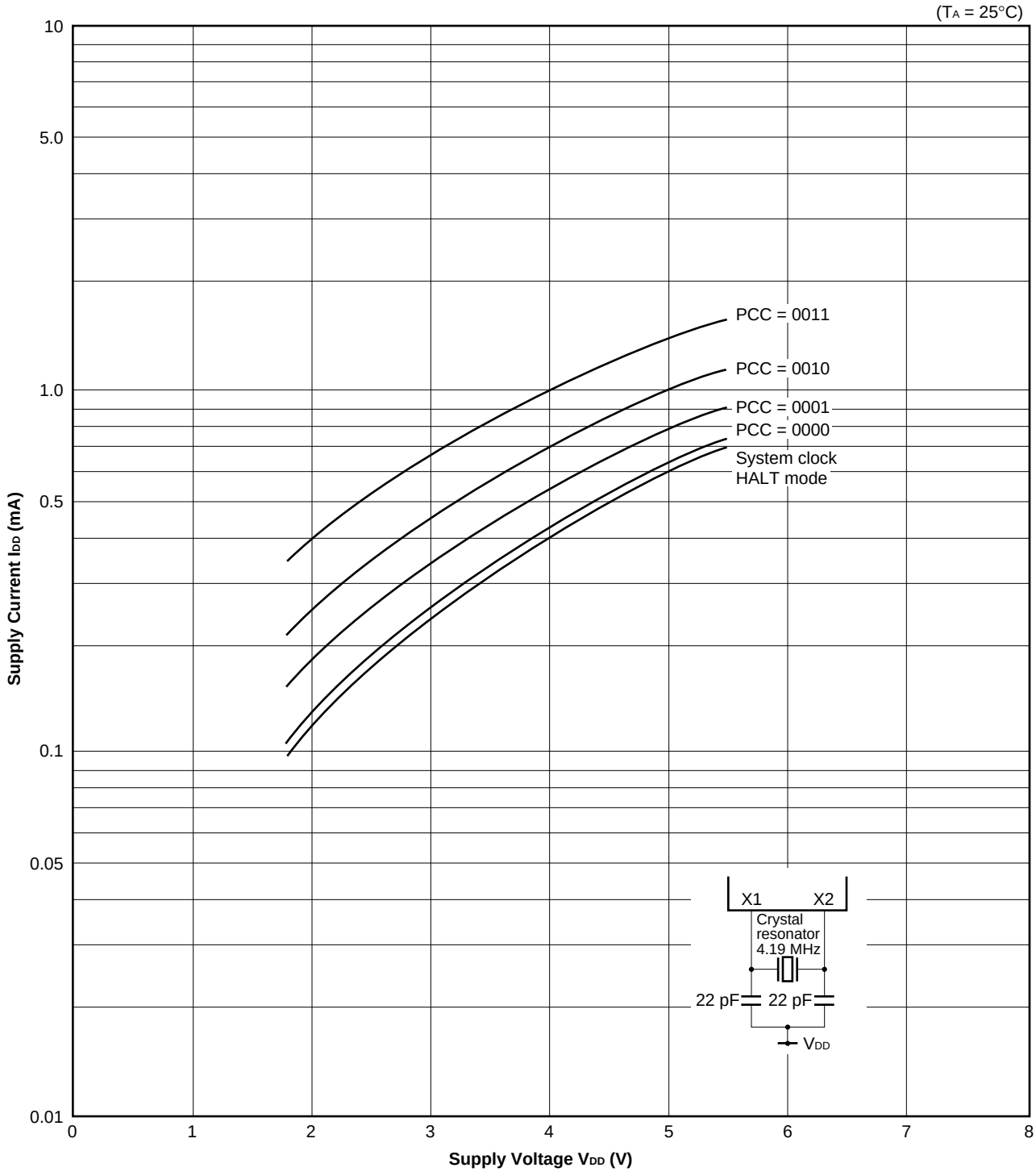


## 13. CHARACTERISTIC CURVES (REFERENCE VALUES)

**$I_{DD}$ vs $V_{DD}$ (System Clock : 6.0-MHz Crystal Resonator)**

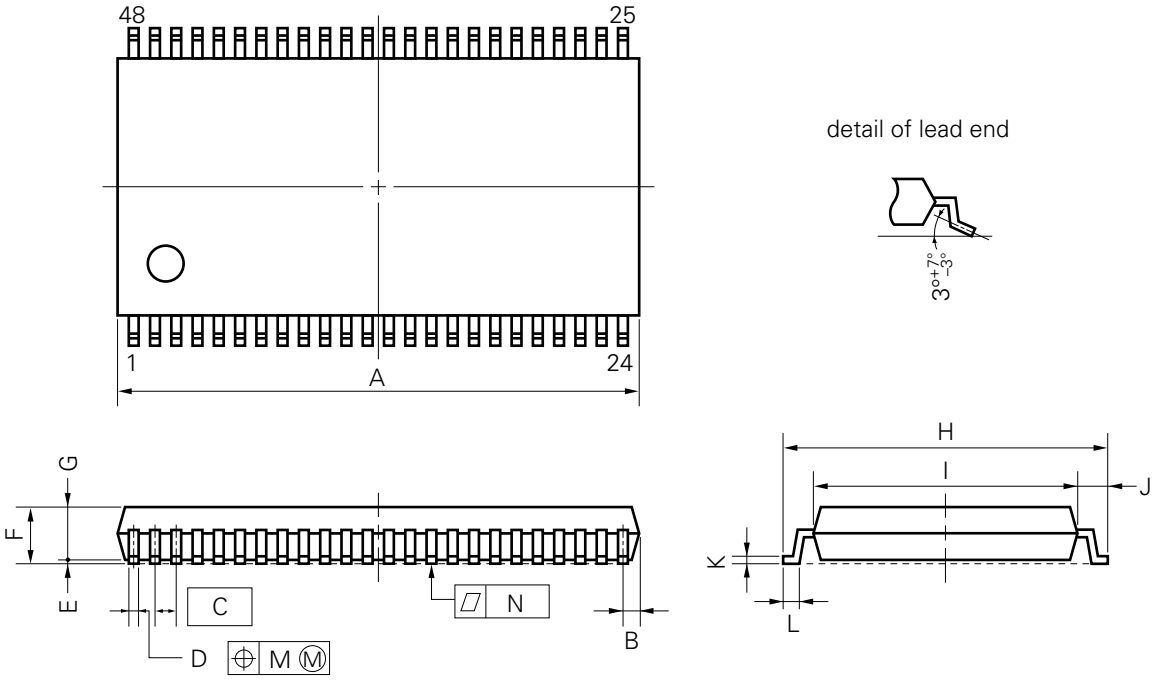


**$I_{DD}$ vs $V_{DD}$ (System Clock : 4.19-MHz Crystal Resonator)**



## 14. PACKAGE DRAWINGS

### 48 PIN PLASTIC SHRINK SOP (375 mil)




P48GT-65-375B-1

**NOTE**

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 16.21 MAX. | 0.639 MAX. |
| B | 0.63 MAX. | 0.025 MAX. |
| C | 0.65 (T.P.) | 0.026 (T.P.) |
| D | 0.30±0.10 | $0.012^{+0.004}_{-0.005}$ |
| E | 0.125±0.075 | 0.005±0.003 |
| F | 2.0 MAX. | 0.079 MAX. |
| G | 1.7±0.1 | 0.067±0.004 |
| H | 10.0±0.3 | $0.394^{+0.012}_{-0.013}$ |
| I | 8.0±0.2 | 0.315±0.008 |
| J | 1.0±0.2 | $0.039^{+0.009}_{-0.008}$ |
| K | $0.15^{+0.10}_{-0.05}$ | $0.006^{+0.004}_{-0.002}$ |
| L | 0.5±0.2 | $0.020^{+0.008}_{-0.009}$ |
| M | 0.10 | 0.004 |
| N | 0.10 | 0.004 |

## 15. RECOMMENDED SOLDERING CONDITIONS

The μPD753208 should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (C10535E).**

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

**Table 15-1. Surface Mounting Type Soldering Conditions**

μPD753204GT-xxx : 48-pin plastic shrink SOP (375 mils, 0.65-mm pitch)
μPD753206GT-xxx : 48-pin plastic shrink SOP (375 mils, 0.65-mm pitch)
μPD753208GT-xxx : 48-pin plastic shrink SOP (375 mils, 0.65-mm pitch)

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared rays reflow | Peak package's surface temperature: 235°C, Reflow time: 30 seconds or less (at 210°C or higher), Number of reflow processes: Twice max. | IR35-00-2 |
| VPS | Peak package's surface temperature: 215°C, Reflow time: 40 seconds or less (at 200°C or higher), Number of reflow processes: Twice max. | VP15-00-2 |
| Wave soldering | Solder temperature: 260°C or below, Flow time: 10 seconds or less, Number of flow process: 1, Preheating temperature: 120°C or below (Package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300°C or below, Time: 3 seconds or less (per device side) | — |

**Caution Use of more than one soldering method should be avoided (except for partial heating).**

## APPENDIX A μPD753108, 753208, AND 75P3216 FUNCTIONAL LIST

| Parameter | | μPD753108 | μPD753208 | μPD75P3216 |
|---|---|---|---|---|
| Program memory | | Mask ROM<br>0000H-1FFFH<br>(8192 × 8 bits) | | One-time PROM<br>0000H-3FFFH<br>(16384 × 8 bits) |
| Data memory | | 000H-1FFH<br>(512 × 4 bits) | | |
| CPU | | 75XL CPU | | |
| Instruction execution time | When main system clock is selected | • 0.95, 1.91, 3.81, 15.3 μs (@ 4.19-MHz operation)<br>• 0.67, 1.33, 2.67, 10.7 μs (@ 6.0-MHz operation) | | |
| | When subsystem clock is selected | 122 μs (@ 32.768-kHz operation) | None | |
| I/O port | CMOS input | 8 (on-chip pull-up resistors can be specified by software: 7) | 6 (on-chip pull-up resistors can be specified by software: 5) | |
| | CMOS input/output | 20 (on-chip pull-up resistors can be specified by software) | | |
| | N-ch open drain input/output | 4 (on-chip pull-up resistors can be specified by software, withstand voltage is 13 V) | | 4 (no mask option, withstand voltage is 13 V) |
| | Total | 32 | 30 | |
| LCD controller/driver | | Segment selection: 16/20/24 (can be changed to CMOS input/output port in 4 time-unit; max. 8) | Segment selection: 4/8/12 segments (can be changed to CMOS input/output port in 4 time-unit; max. 8) | |
| | | Display mode selection: static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias) | | |
| | | On-chip split resistor for LCD driver can be specified by using mask option. | | No on-chip split resistor for LCD driver |
| Timer | | 5 channels<br>• 8-bit timer/event counter: 3 channels<br>• Basic interval timer/ watchdog timer: 1 channel<br>• Watch timer: 1 channel | 5 channels<br>• 8-bit timer counter: 2 channels (can be used as the 16-bit timer counter, carrier generator, and timer with gate)<br>• 8-bit timer/event counter: 1 channel<br>• Basic interval timer/watchdog timer: 1 channel<br>• Watch timer: 1 channel | |
| Clock output (PCL) | | • Φ, 524, 262, 65.5 kHz (Main system clock: @ 4.19-MHz operation)<br>• Φ, 750, 375, 93.8 kHz (Main system clock: @ 6.0-MHz operation) | | |
| Buzzer output (BUZ) | | • 2, 4, 32 kHz (Main system clock: @ 4.19-MHz operation or sub-system clock: @ 32.768-kHz operation)<br>• 2.86, 5.72, 45.8 kHz (Main system clock: @ 6.0-MHz operation) | • 2, 4, 32 kHz (Main system clock: @ 4.19-MHz operation)<br>• 2.93, 5.86, 46.9 kHz (Main system clock: @ 6.0-MHz operation) | |
| Serial interface | | 3 modes are available<br>• 3-wire serial I/O mode ... MSB/LSB can be selected for transfer top bit<br>• 2-wire serial I/O mode<br>• SBI mode | | |
| SCC register | | Contained | None | |
| SOS register | | | | |
| Vectored interrupt | | External: 3, internal: 5 | External: 2, internal: 5 | |

| Parameter | μPD753108 | μPD753208 | μPD75P3216 |
|---|---|---|---|
| Test input | External: 1, internal: 1 | | |
| Operation supply voltage | $V_{DD}$ = 1.8 to 5.5 V | | |
| Operating ambient temperature | $T_A$ = –40 to +85°C | | |
| Package | • 64-pin plastic QFP (14 × 14 mm)<br>• 64-pin plastic QFP (12 × 12 mm) | • 48-pin plastic shrink SOP (375 mils, 0.65-mm pitch) | |

## APPENDIX B DEVELOPMENT TOOLS

The following development tools are provided for system development using the μPD753208.

In 75XL series, the relocatable assembler which is common to the μPD753208 Subseries is used in combination with the device file of each product.

**Language processor**

| | | | | |
|---|---|---|---|---|
| RA75X relocatable assembler | Host machine | OS | Distribution media | Part number (product name) |
| | PC-9800 series | MS-DOS™ Ver. 3.30 to Ver. 6.2 Note | 3.5-inch 2HD | μS5A13RA75X |
| | | | 5-inch 2HD | μS5A10RA75X |
| | IBM PC/AT™ and compatible machines | Refer to **section** "**OS for IBM PC**" | 3.5-inch 2HC | μS7B13RA75X |
| | | | 5-inch 2HC | μS7B10RA75X |

| | | | | |
|---|---|---|---|---|
| Device file | Host machine | OS | Distribution media | Part number (product name) |
| | PC-9800 series | MS-DOS Ver. 3.30 to Ver. 6.2 Note | 3.5-inch 2HD | μS5A13DF753208 |
| | | | 5-inch 2HD | μS5A10DF753208 |
| | IBM PC/AT and compatible machines | Refer to **section** "**OS for IBM PC**" | 3.5-inch 2HC | μS7B13DF753208 |
| | | | 5-inch 2HC | μS7B10DF753208 |

**PROM write tools**

| | | | | |
|---|---|---|---|---|
| Hardware | PG-1500 | PG-1500 is a PROM programmer which enables you to program single chip microcomputers including PROM by stand-alone or host machine operation by connecting an attached board and optional programmer adapter to PG-1500. It also enables you to program typical PROM devices of 256 Kbits to 4 Mbits. | | |
| | PA-75P3216GT | PROM programmer adapter for the μPD75P3216GT. Connect the programmer adapter to PG-1500 for use. | | |
| Software | PG-1500 controller | PG-1500 and a host machine are connected by serial and parallel interfaces and PG-1500 is controlled on the host machine. | | |
| | | Host machine / OS | Distribution media | Part number (product name) |
| | | PC-9800 series / MS-DOS Ver. 3.30 to Ver. 6.2 Note | 3.5-inch 2HD | μS5A13PG1500 |
| | | | 5-inch 2HD | μS5A10PG1500 |
| | | IBM PC/AT and compatible machines / Refer to **section** "**OS for IBM PC**" | 3.5-inch 2HD | μS7B13PG1500 |
| | | | 5-inch 2HC | μS7B10PG1500 |

**Note** Ver. 5.00 or later have the task swap function, but it cannot be used for this software.

**Remarks 1.** Operation of the assembler and device file is guaranteed only on the above host machine and OSs.

**2.** Operation of the PG-1500 controller is guaranteed only on the above host machine and OSs.

**Debugging tool**

The in-circuit emulators (IE-75000-R and IE-75001-R) are available as the program debugging tool for the μPD753208.

The system configurations are described as follows.

<table>
<tr><td rowspan="5">Hardware</td><td>IE-75000-R Note 1</td><td colspan="4">In-circuit emulator for debugging the hardware and software when developing the application systems that use the 75X series and 75XL series. When developing a μPD753208 subseries, the emulation board IE-75300-R-EM and emulation probe EP-753208GT-R that are sold separately must be used with the IE-75000-R.<br>By connecting with the host machine and the PROM programmer, efficient debugging can be made.<br>It contains the emulation board IE-75000-R-EM which is connected.</td></tr>
<tr><td>IE-75001-R</td><td colspan="4">In-circuit emulator for debugging the hardware and software when developing the application systems that use the 75X series and 75XL series. When developing a μPD753208 subseries, the emulation board IE-75300-R-EM and emulation probe EP-753208GT-R which are sold separately must be used with the IE-75001-R.<br>It can debug the system efficiently by connecting the host machine and PROM programmer.</td></tr>
<tr><td>IE-75300-R-EM</td><td colspan="4">Emulation board for evaluating the application systems that use a μPD753208 subseries.<br>It must be used with the IE-75000-R or IE-75001-R.</td></tr>
<tr><td>EP-753208GT-R<br>EV-9500GF-48</td><td colspan="4">Emulation probe for the μPD753208GT.<br>It must be connected to the IE-75000-R (or IE-75001-R) and IE-75300-R-EM.<br>It is supplied with the 48-pin conversion adapter EV-9500GF-48 which facilitates connection to a target system.</td></tr>
<tr><td rowspan="4">Software</td><td rowspan="4">IE control program</td><td colspan="4">Connects the IE-75000-R or IE-75001-R to a host machine via RS-232-C and Centronix I/F and controls the above hardware on a host machine.</td></tr>
<tr><td rowspan="2">Host machine</td><td colspan="2" rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part No.<br>(product name)</td></tr>
<tr></tr>
<tr><td>PC-9800 series</td><td colspan="2">MS-DOS<br>(Ver. 3.30 to Ver. 6.2 Note 2)</td><td>3.5-inch 2HD<br>5-inch 2HD</td><td>μS5A13IE75X<br>μS5A10IE75X</td></tr>
<tr><td>IBM PC/AT and its compatible machine</td><td colspan="2">Refer to section “OS for IBM PC”</td><td>3.5-inch 2HC<br>5-inch 2HC</td><td>μS7B13IE75X<br>μS7B10IE75X</td></tr>
</table>

**Notes 1.** Maintenance parts.

**2.** Ver. 5.00 or later have the task swap function, but it cannot be used for this software.

**Remarks 1.** Operation of the IE control program is guaranteed only on the above host machines and OSs.

**2.** The μPD753204, 753206, 753208, and 75P3216 are commonly referred to as the μPD753208 Subseries.

**OS for IBM PC**

The following IBM PC OS's are supported.

| OS | Version |
|---|---|
| PC DOS™ | Ver. 5.02 to Ver. 6.3<br>J6.1/V Note to J6.3/V Note |
| MS-DOS | Ver. 5.0 to Ver. 6.22<br>5.0/V Note to 6.2/V Note |
| IBM DOS™ | J5.02/V Note |

**Note** English version is supported.

**Caution Ver. 5.0 and later have the task swap function, but it cannot be used for this software.**

## APPENDIX C RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

**Documents related to device**

| Document Name | Document No. | |
|---|---|---|
| | Japanese | English |
| μPD753204, 753206, 753208 Data Sheet | U10166J | This manual |
| μPD75P3216 Data Sheet | U10241J | U10241E |
| μPD753208 User's Manual | U10158J | U10158E |
| 75XL Series Selection Guide | U10453J | U10453E |

**Documents related to development tool**

| Document Name | | | Document No. | |
|---|---|---|---|---|
| | | | Japanese | English |
| Hardware | IE-75000-R/IE-75001-R User's Manual | | EEU-846 | EEU-1416 |
| | IE-75300-R-EM User's Manual | | U11354J | U11354E |
| | EP-753208GT-R User's Manual | | U10739J | U10739E |
| | PG-1500 User's Manual | | U11940J | EEU-1335 |
| Software | RA75X Assembler Package User's Manual | Operation | EEU-731 | EEU-1346 |
| | | Language | EEU-730 | EEU-1363 |
| | PG-1500 Controller User's Manual | PC-9800 Series (MS-DOS) Base | EEU-704 | EEU-1291 |
| | | IBM PC Series (PC DOS) Base | EEU-5008 | U10540E |

**Other related documents**

| Document Name | Document No. | |
|---|---|---|
| | Japanese | English |
| Semiconductor Device Package Manual | C10943X | |
| Semiconductor Device Mounting Technology Manual | C10535J | C10535E |
| Quality Grades on NEC Semiconductor Devices | C11531J | C11531E |
| NEC Semiconductor Device Reliability/Quality Control System | C10983J | C10983E |
| Electrostatic Discharge (ESD) Test | MEM-539 | IEI-1201 |
| Guide to Quality Assurance for Semiconductor Devices | C11893J | MEI-1202 |
| Microcontroller – Related Product Guide – Third Party Products – | C11416J | – |

**Caution The contents of the documents listed above are subject to change without prior notice to users. Make sure to use the latest edition when starting design.**

# NOTES FOR CMOS DEVICES

## ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.**

## ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.**

## ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.**

# Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

**NEC Electronics Inc. (U.S.)**
Santa Clara, California
Tel: 800-366-9782
Fax: 800-729-9288

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Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

**NEC Electronics (UK) Ltd.**
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

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Tel: 040-2445845
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Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

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Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

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Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

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Hong Kong
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Fax: 2886-9022/9044

**NEC Electronics Hong Kong Ltd.**
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

**NEC Electronics Singapore Pte. Ltd.**
United Square, Singapore 1130
Tel: 253-8311
Fax: 250-3583

**NEC Electronics Taiwan Ltd.**
Taipei, Taiwan
Tel: 02-719-2377
Fax: 02-719-5951

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Sao Paulo-SP, Brasil
Tel: 011-889-1680
Fax: 011-889-1689

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- Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
- Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
- Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.

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